IGLOO nano Low Power Flash FPGAs with Flash*Freeze Technology

INTRODUCTION

The IGLOO® family of Flash FPGAs, based on a 130-nm Flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, re-programmability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO nano devices enables entering and exiting an ultra-low power mode that consumes nanoPower while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption while the IGLOO nano device is completely functional in the system. This allows the IGLOO nano device to control system power management based on external inputs (that is, scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile Flash technology gives IGLOO nano devices the advantage of being a secure, low power, single-chip solution that is Instant On. The IGLOO nano device is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO nano devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated Phase-locked Loop (PLL). The AGLN020 and smaller devices have no PLL or RAM support. IGLOO nano devices have up to 250 k system gates, supported with up to 36 kbits of true dual-port SRAM and up to 71 user I/Os.

IGLOO nano devices increase the breadth of the IGLOO product line by adding new features and packages for greater customer value in high volume consumer, portable, and battery-backed markets. Features such as smaller footprint packages designed with two-layer PCBs in mind, power consumption measured in nanoPower, Schmitt trigger, and bus hold (hold previous I/O state in Flash*Freeze mode) functionality make these devices ideal for deployment in applications that require high levels of flexibility and low cost.

Features

The following is a list of features supported:

- Low Power
  - nanoPower Consumption—Industry's Lowest Power
  - 1.2V to 1.5V Core Voltage Support for Low Power
  - Supports Single-Voltage System Operation
  - Low Power Active FPGA Operation
  - Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
  - Easy Entry to/exit from Ultra-Low Power Flash*Freeze Mode
- Small Footprint Packages
  - As Small as 3 x 3 mm in Size
- Wide Range of Features
  - 10,000 to 250,000 System Gates
  - Up to 36 kbits of True Dual-Port SRAM
  - Up to 71 User I/Os
- Reprogrammable Flash Technology
  - 130-nm, 7-Layer Metal, Flash-Based CMOS Process
  - Instant On Level 0 Support

- Single-Chip Solution
- Retains Programmed Design When Powered Off
- 250 MHz (1.5V systems) and 160 MHz (1.2V systems) System Performance

- In-System Programming (ISP) and Security
  - ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption through JTAG (IEEE® 1532–compliant)
  - FlashLock® Designed to Secure FPGA Contents
  - 1.2V Programming
- High-Performance Routing Hierarchy
  - Segmented, Hierarchical Routing and Clock Structure
- Advanced I/Os
  - 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V Mixed-Voltage Operation
  - Bank-Selectable I/O Voltages—up to 4 Banks per Chip
  - Single-Ended I/O Standards: LVTTL, LVCMOS 3.3V/2.5V/1.8V/1.5V/1.2V
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7V to 3.6V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14V to 1.575V
- I/O Registers on Input, Output, and Enable Paths
- Selectable Schmitt Trigger Inputs
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO Family

Clock Conditioning Circuit (CCC) and PLL

- Up to Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)
- True Dual-Port SRAM (except × 18 organization)[1]

Enhanced Commercial Temperature Range

- Tj = -20 °C to +85 °C

TABLE 1: IGLOO NANO CHARACTERISTICS

IGLOO nano Devices	AGLN010	AGLN015[1]	AGLN020	AGLN060	AGLN125	AGLN250
System Gates	10,000	15,000	20,000	60,000	125,000	250,000
Typical Equivalent Macrocells	86	128	172	512	1,024	2,048
VersaTiles (D-flip-flops)	260	384	520	1,536	3,072	6,144
Flash*Freeze Mode (typical, µW)	2	4	4	10	16	24
RAM Kbits (1,024 bits)[2]	—	—	—	18	36	36
4,608-Bit Blocks[2]	—	—	—	4	8	8

TABLE 1: IGLOO NANO CHARACTERISTICS

IGLOO nano Devices	AGLN010	AGLN015[1]	AGLN020	AGLN060	AGLN125	AGLN250
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1
Secure (AES) ISP[2]	—	—	—	Yes	Yes	Yes
Integrated PLL in CCCs [2,3]	—	—	—	1	1	1
VersaNet Globals	4	4	4	18	18	18
I/O Banks	2	3	3	2	2	4
Maximum User I/Os (packaged device)	34	49	52	71	71	68
Maximum User I/Os (Known Good Die)	34	—	52	71	71	68
Package Pins UC/CS QFN VQFP	 UC36 QN48	 QN68	 UC81[5], CS81 QN68	 CS81 VQ100	 CS81 VQ100	 CS81 VQ100

Note 1: Not recommended for new designs (CN1203).

2: AGLN020 and smaller devices do not support this feature.

3: AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs.

4: For higher densities and support of additional features, see the *IGLOO Low Power Flash FPGAs with Flash*Freeze Technology*.

5: Package UC81 has been discontinued.

I/Os Per Package

TABLE 2: I/OS PER PACKAGE

IGLOO nano Devices	AGLN010	AGLN015[1]	AGLN020	AGLN060	AGLN125	AGLN250
Known Good Die	34	–	52	71	71	68
UC36	23	—	—	—	—	—
QN48	34	—	—	—	—	—
QN68	—	49	49	—	—	—
UC81	—	—	52[5]	—	—	—
CS81	—	—	52	60	60	60
VQ100	—	—	—	71	71	68

Note 1: Not recommended for new designs.

2: For higher densities and support of additional features, see the *IGLOO Low Power Flash FPGAs with Flash*Freeze Technology*.

3: When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.

4: "G" indicates RoHS-compliant packages. Refer to *"IGLOO nano Ordering Information"* for the location of the "G" in the part number. For nano devices, the VQ100 package is offered in both leaded and RoHS-compliant versions. All other packages are RoHS-compliant only.

5: Package UC81 has been discontinued.

TABLE 3: IGLOO NANO FPGAS PACKAGE SIZES DIMENSIONS

Packages	UC36	UC81[1]	CS81	QN48	QN68	VQ100
Length × Width (mm\mm)	3 x 3	4 x 4	5 x 5	6 x 6	8 x 8	14 x 14

TABLE 3: IGLOO NANO FPGAS PACKAGE SIZES DIMENSIONS

Packages	UC36	UC81[1]	CS81	QN48	QN68	VQ100
Nominal Area (mm^2)	9	16	25	36	64	196
Pitch (mm)	0.4	0.4	0.5	0.4	0.4	0.5
Height (mm)	0.80	0.80	0.80	0.90	0.90	1.20

Note 1: Package UC81 has been discontinued.

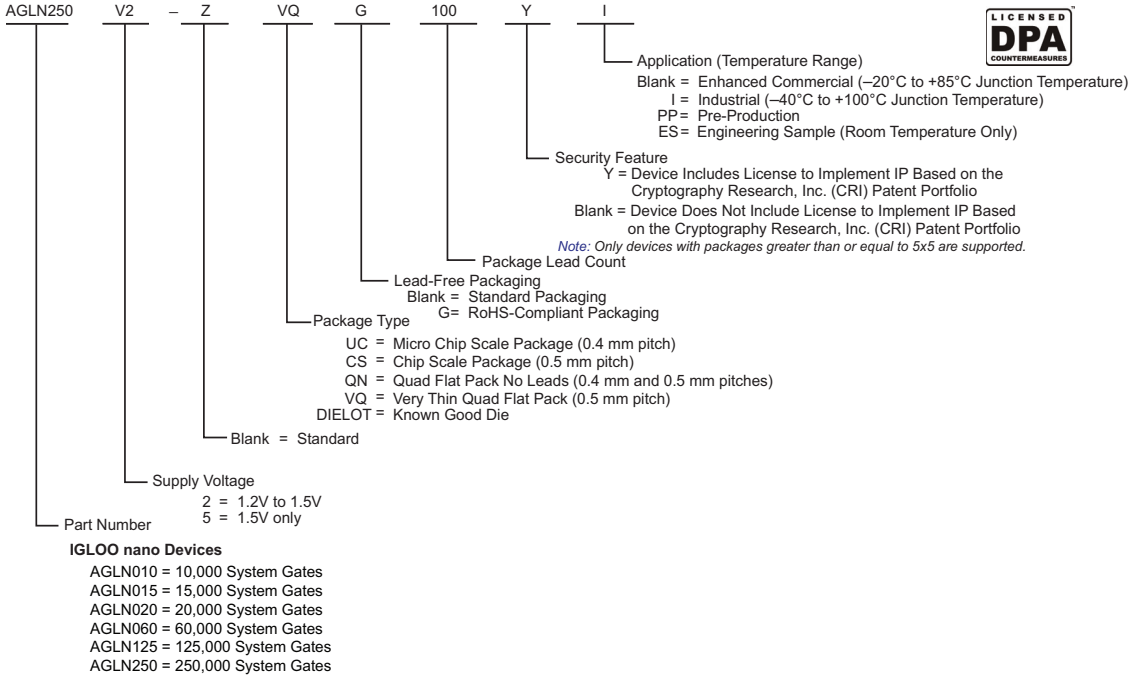
IGLOO nano Device Status

TABLE 4: IGLOO NANO DEVICE STATUS

IGLOO nano Devices	Status
AGLN010	Production
AGLN015	Not recommended for new designs.
AGLN020	Production
AGLN060	Production
AGLN125	Production
AGLN250	Production

IGLOO nano Ordering Information

FIGURE 1: ORDERING INFORMATION



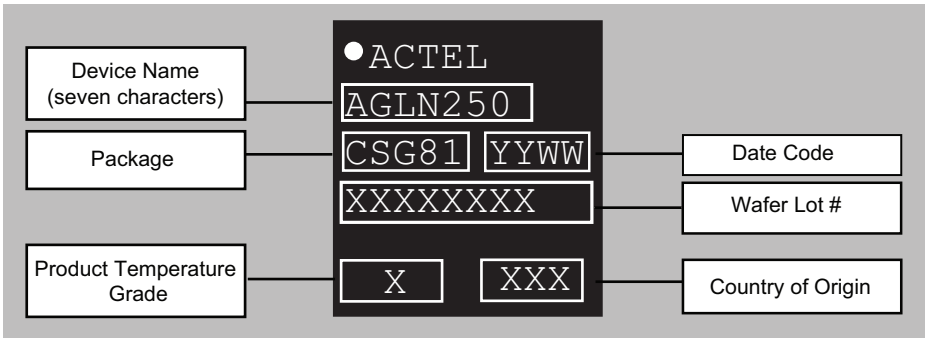
Note: Marking Information: IGLOO nano V2 devices do not have a V2 marking, but IGLOO nano V5 devices are marked with a V5 designator.

Device Marking

Microchip normally topside marks the full ordering part number on each device. There are some exceptions to this, such as the V2 designator for IGLOO devices and packages where space is physically limited. Packages that have limited characters available are UC36, CS81, QN48, QN68, and QFN132. On these specific packages, a subset of the device marking will be used that includes the required legal information and as much of the part number as allowed by character limitation of the device. In this case, devices will have a truncated device marking and may exclude the applications markings, such as the I designator for Industrial Devices or the ES designator for Engineering Samples.

The following figure shows an example of device marking based on the AGLN250V2-CSG81. The actual mark will vary by the device/package combination ordered.

FIGURE 2: EXAMPLE OF DEVICE MARKING FOR SMALL FORM FACTOR PACKAGES



Temperature Grade Offerings

In the following table:

- C = enhanced commercial temperature range: –20 °C to +85 °C junction temperature
- I = industrial temperature range: –40 °C to +100 °C junction temperature

TABLE 5: TEMPERATURE GRADE OFFERINGS

Package	AGLN010	AGLN015[1]	AGLN020	AGLN060	AGLN125	AGLN250
UC36	C, I	—	—	—	—	—
QN48	C, I	—	—	—	—	—
QN68	—	C, I	C, I	—	—	—
UC81[2]	—	—	C, I	—	—	—
CS81	—	—	C, I	C, I	C, I	C, I
VQ100	—	—	—	C, I	C, I	C, I

Note 1: Not recommended for new designs.

2: Package UC81 has been discontinued.

Contact your local Microchip representative for device availability: *https://www.microchip.com/en-us/about/global-sales-and-distribution*.

Contents

1.0 IGLOO NANO DEVICE OVERVIEW

1.1 Flash*Freeze Technology

The IGLOO nano device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO nano devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO nano V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

During Flash*Freeze mode, each I/O can be set to the following configurations: hold previous state, tristate, HIGH, or LOW.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and small-footprint packages make IGLOO nano devices the best fit for portable electronics.

1.1.1 FLASH ADVANTAGES

1.1.1.1 Low Power

Flash-based IGLOO nano devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO nano devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO nano devices also have low dynamic power consumption to further maximize power savings; power is reduced even further by the use of a 1.2V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO nano device the lowest total system power offered by any FPGA.

1.1.1.2 Security

Nonvolatile, Flash-based IGLOO nano devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO nano devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile Flash programming can offer.

IGLOO nano devices utilize a 128-bit Flash-based lock and a separate AES key to provide the highest level of security in the FPGA industry for programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO nano devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO nano devices have a built-in AES decryption engine and a Flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO nano devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of IGLOO nano devices. The Flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. IGLOO nano devices, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO nano device provides the best available security for programmable logic designs.

1.1.1.3 Single Chip

Flash-based FPGAs store their configuration information in on-chip Flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, Flash-based IGLOO nano FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

1.1.1.4 Instant On

Microchip Flash-based IGLOO nano devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of Flash-based IGLOO nano devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO nano device's Flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brown-out detection, and clock generator devices from the PCB design. Flash-based IGLOO nano devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO nano Flash FPGAs enable the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs, the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

1.1.1.5 Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO nano devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic.

Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO nano device architecture mitigates the need for ASIC migration at higher user volumes. This makes IGLOO nano devices cost-effective ASIC replacement solutions, especially for applications in the consumer, networking/communications, computing, and avionics markets.

With a variety of devices under $1, IGLOO nano FPGAs enable cost-effective implementation of programmable logic and quick time to market.

1.1.1.6 Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO nano Flash-based FPGAs. Once it is programmed, the Flash cell configuration element of IGLOO nano FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

1.1.1.7 Advanced Flash Technology

The IGLOO nano device offers many benefits, including nonvolatility and reprogrammability, through an advanced Flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant Flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO nano FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

1.1.1.8 Advanced Architecture

The proprietary IGLOO nano architecture provides granularity comparable to standard-cell ASICs. The IGLOO nano device consists of five distinct and programmable architectural features (Figure 1-3 to Figure 1-3):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate Flash switch interconnections. The versatility of the IGLOO nano core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC® family of third-generation-architecture FlashFlash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

FIGURE 1-1: IGLOO DEVICE ARCHITECTURE OVERVIEW WITH TWO I/O BANKS AND NO RAM (AGLN010)

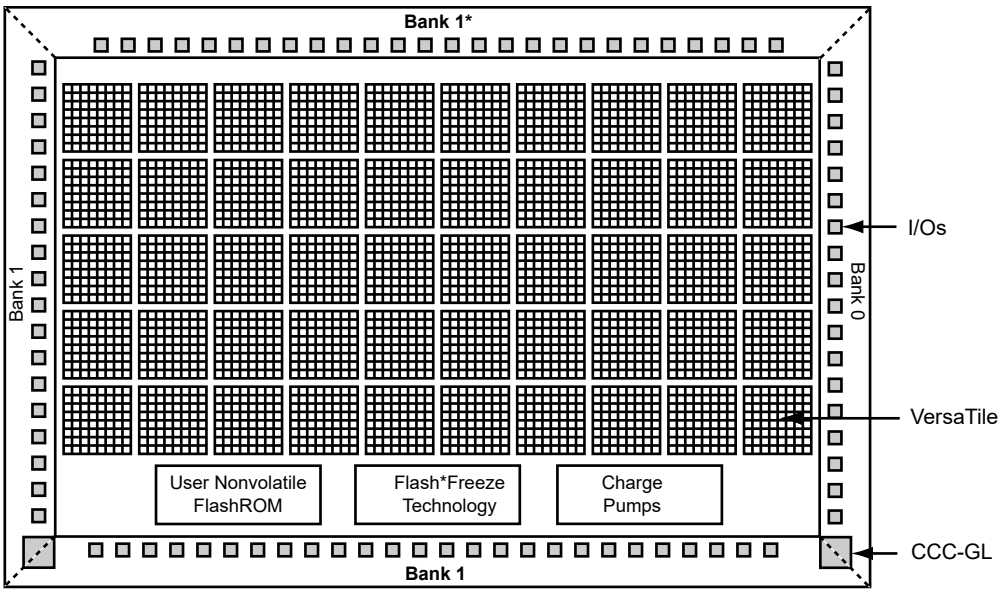


FIGURE 1-2: IGLOO DEVICE ARCHITECTURE OVERVIEW WITH THREE I/O BANKS AND NO RAM (AGLN015 AND AGLN020)

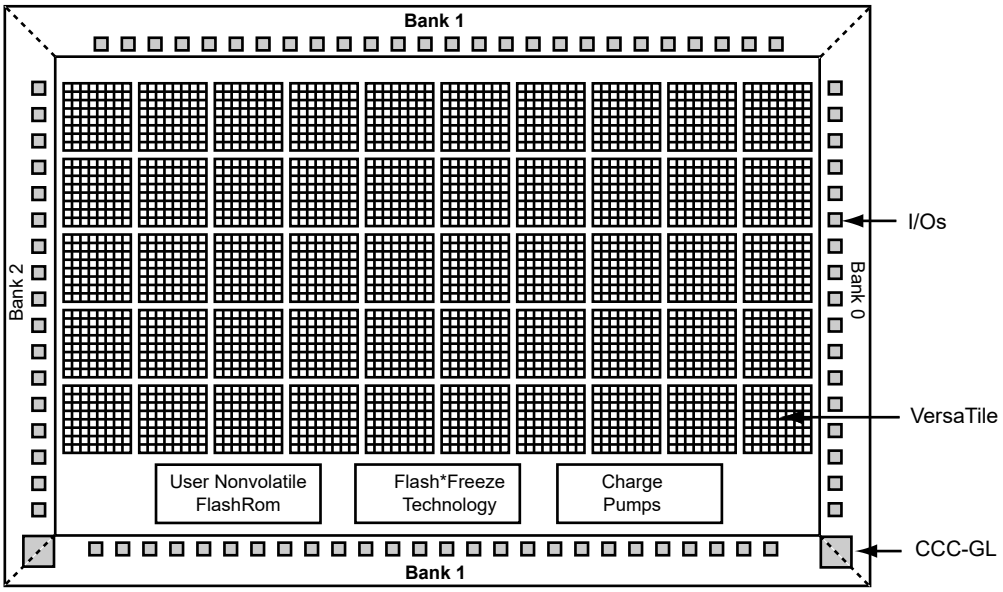


FIGURE 1-3: IGLOO DEVICE ARCHITECTURE OVERVIEW WITH TWO I/O BANKS (AGLN060, AGLN125)

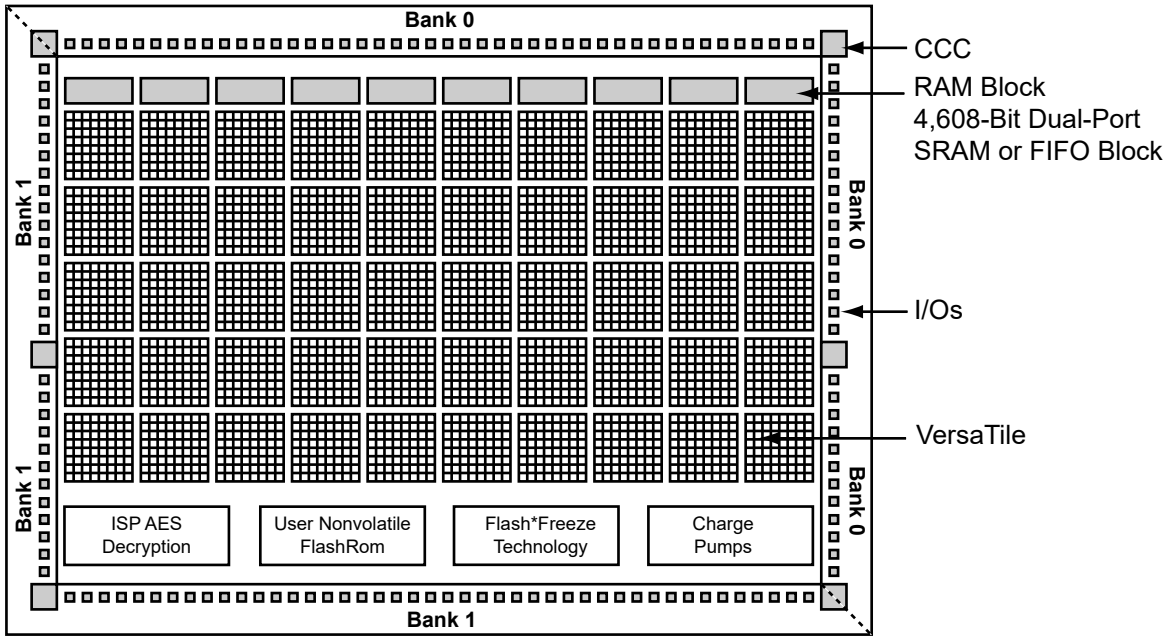
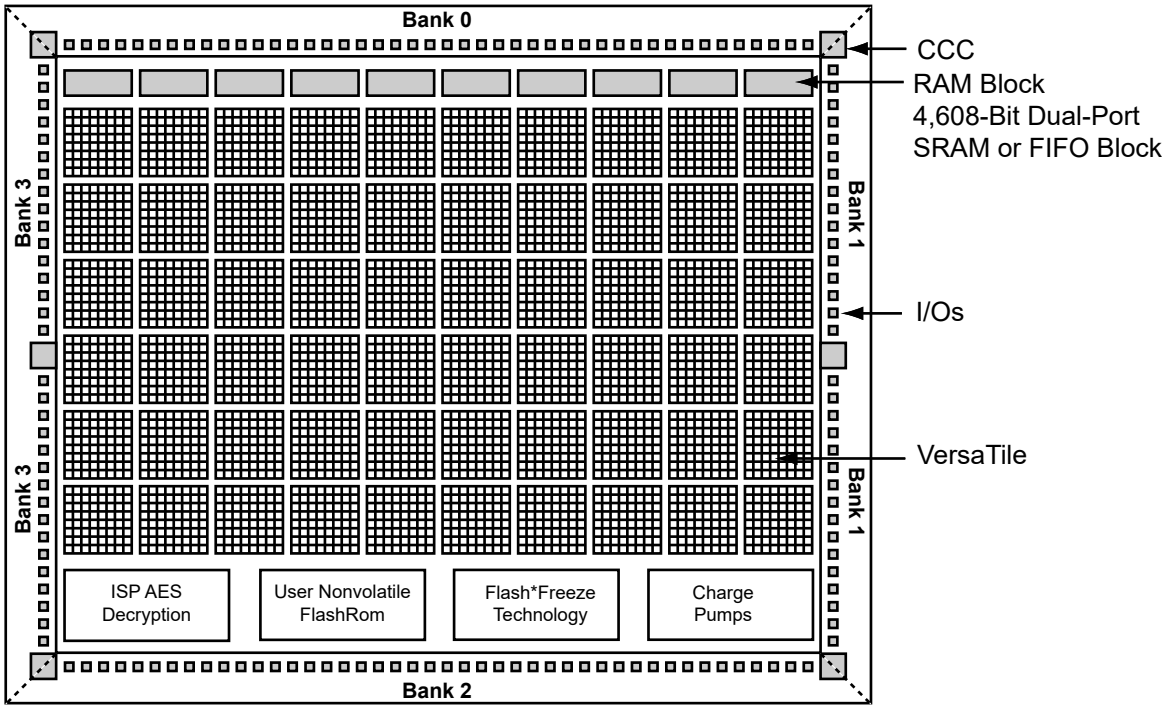


FIGURE 1-4: IGLOO DEVICE ARCHITECTURE OVERVIEW WITH FOUR I/O BANKS (AGLN250)



1.2 Flash*Freeze Technology

The IGLOO nano device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at

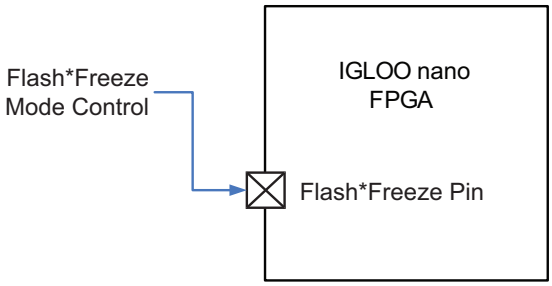
their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode.

Alternatively, I/Os can be set to a specific state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 2 µW in this mode.

Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. For an illustration of entering/exiting Flash*Freeze mode, see the following figure. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned.

FIGURE 1-5: IGLOO NANO FLASH*FREEZE MODE



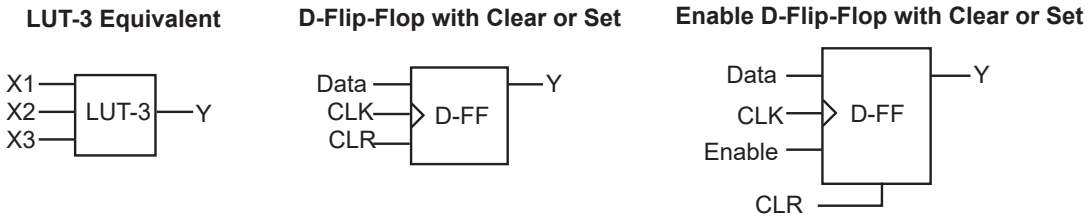
1.2.1 VERSATILES

The IGLOO nano core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The IGLOO nano VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

For VersaTile configurations. see the following figure.

FIGURE 1-6: VERSATILE CONFIGURATIONS



1.2.2 USER NONVOLATILE FLASHROM

IGLOO nano devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO nano IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGLN020 and smaller devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed through the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or through direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The IGLOO nano development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature enables the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Microchip Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

1.2.3 SRAM AND FIFO

IGLOO nano devices (except the AGLN020 and smaller devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256 × 18, 512 × 9, 1k × 4, 2k × 2, and 4k × 1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized through the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGLN020 and smaller devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

1.2.4 PLL AND CCC

Higher density IGLOO nano devices using either the two I/O bank or four I/O bank architectures provide designers with very flexible clock conditioning capabilities. AGLN060, AGLN125, and AGLN250 contain six CCCs. One CCC (center west side) has a PLL. The AGLN020 and smaller devices use different CCCs in their architecture (CCC-GL). These CCC-GLs contain a global MUX but do not have any PLLs or programmable delays.

For devices using the six CCC block architecture, these are located at the four corners and the centers of the east and west sides. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from dedicated connections to the CCC block, which are located near the CCC.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)

- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC} (for PLL only)

1.2.4.1 Global Clocking

IGLOO nano devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core through multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

1.2.5 I/OS WITH ADVANCED I/O STANDARDS

IGLOO nano FPGAs feature a flexible I/O structure, supporting a range of voltages (1.2V, 1.2V wide range, 1.5V, 1.8V, 2.5V, 3.0V wide range, and 3.3V).

The I/Os are organized into banks with two, three, or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of various single-data-rate applications for all versions of nano devices and double-data-rate applications for the AGLN060, AGLN125, and AGLN250 devices.

IGLOO nano devices support LVTTL and LVCMOS I/O standards, are hot-swappable, and support cold-sparing and Schmitt trigger.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

1.3 Wide Range I/O Support

IGLOO nano devices support JEDEC-defined wide range I/O operation. IGLOO nano devices support both the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7V to 3.6V, and JESD8-12 with its 1.2V nominal, supporting an effective operating range of 1.14V to 1.575V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

1.4 Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-7).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

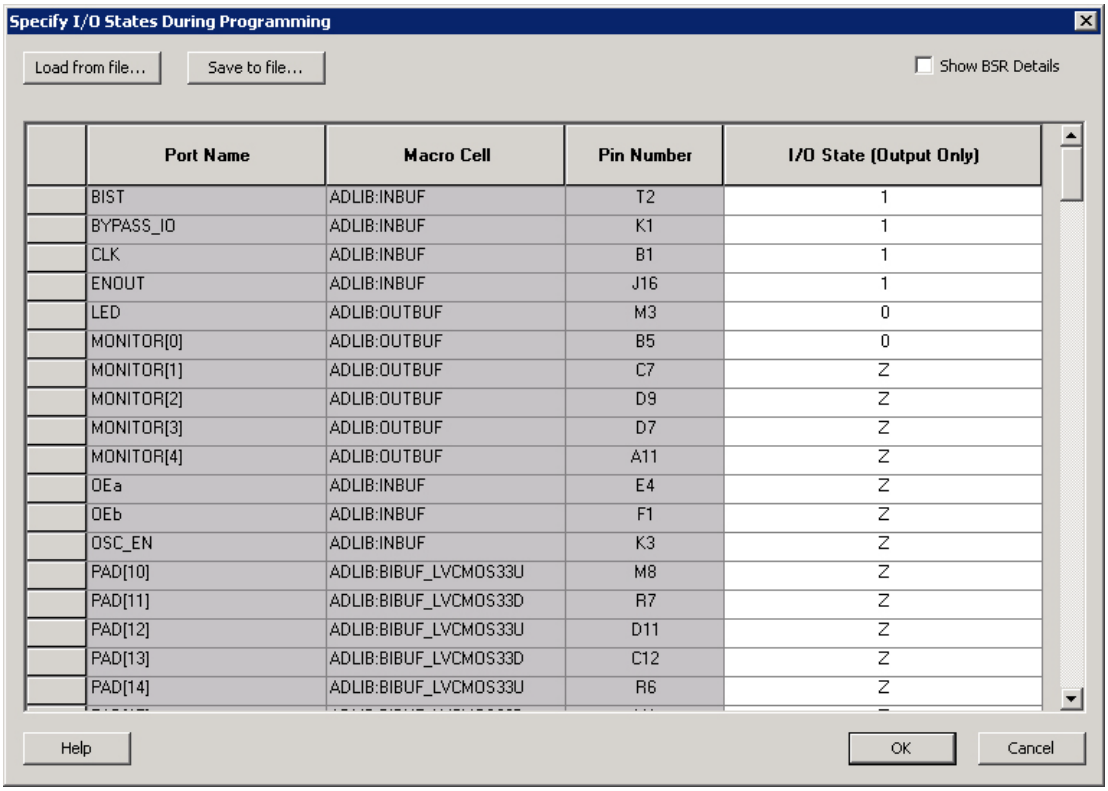
   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

FIGURE 1-7: I/O STATES DURING PROGRAMMING WINDOW



6. Click **OK** to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2.0 IGLOO NANO DC AND SWITCHING CHARACTERISTICS

2.1 General Specifications

The Z feature grade does not support the enhanced nano features of Schmitt trigger input, Flash*Freeze bus hold (hold previous I/O state in Flash*Freeze mode), cold-sparing, and hot-swap I/O capability. For more information, see "IGLOO nano Ordering Information" .

2.1.1 OPERATING CONDITIONS

Stresses beyond those listed in the following table may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 is not implied.

TABLE 2-1: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI[1]	I/O input voltage	–0.3 V to 3.6V	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Note 1: The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4.

2: For Flash programming and retention maximum limits, see Table 2-3, and for recommended operating limits, see Table 2-2.

TABLE 2-2: RECOMMENDED OPERATING CONDITIONS [1]

Symbol	Parameter		Extended Commercial	Industrial	Units
T_J	Junction temperature		–20 to + 85[2]	–40 to +100[2]	°C
VCC	1.5V DC core supply voltage[3]		1.425 to 1.575	1.425 to 1.575	V
	1.2V–1.5V wide range core voltage[4,5]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP [6]	Programming voltage	Programming mode	3.15 to 3.45	3.15 to 3.45	V
		Operation	0 to 3.6	0 to 3.6	V
VCCPLL[7]	Analog power supply (PLL)	1.5V DC core supply voltage[3]	1.425 to 1.575	1.425 to 1.575	V
		1.2V–1.5V wide range core supply voltage[4]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [8,9]	1.2V DC supply voltage [4]		1.14 to 1.26	1.14 to 1.26	V
	1.2V DC wide range supply voltage [4]		1.14 to 1.575	1.14 to 1.575	V
	1.5V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3V DC wide range supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V

Note 1: All parameters representing voltages are measured with respect to GND unless otherwise specified.

2: Default Junction Temperature Range in the Libero SoC software is set to 0 °C to +70 °C for commercial, and -40 °C to +85 °C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microchip recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, see the New Project Dialog Box in the Libero Online Help.

3: For IGLOO® nano V5 devices

4: For IGLOO nano V2 devices only, operating at VCCI ≥ VCC

5: IGLOO nano V5 devices can be programmed with the VCC core voltage at 1.5V only. IGLOO nano V2 devices can be programmed with the VCC core voltage at 1.2V (with FlashPro4 only) or 1.5V. If you are using FlashPro3 and want to do in-system programming using 1.2V, please contact the factory.

6: V_{PUMP} can be left floating during operation (not programming mode).

7: VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter for further information.

8: VMV pins must be connected to the corresponding VCCI pins. See the Pin Descriptions chapter of the IGLOO nano FPGA Fabric User's Guide for further information.

9: The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-21. VCCI should be at the same voltage within a given I/O bank.

10: 3.3V wide range is compliant to the JESD8-B specification and supports 3.0V VCCI operation.

TABLE 2-3: FLASH PROGRAMMING LIMITS – RETENTION, STORAGE, AND OPERATING TEMPERATURE[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Note 1: This is a stress rating only; functional operation at any condition other than those indicated is not implied.

2: These limits apply for program/data retention only. Refer to Table 2-1 and Table 2-2 for device operating conditions and absolute limits.

TABLE 2-4: OVERSHOOT AND UNDERSHOOT LIMITS [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7V or less	10%	1.4V
	5%	1.49V
3V	10%	1.1V
	5%	1.19V
3.3V	10%	0.79V
	5%	0.88V
3.6V	10%	0.45V
	5%	0.54V

Note 1: Based on reliability requirements at 85 °C.

2: The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15V.

2.1.2 I/O POWER-UP AND SUPPLY VOLTAGE THRESHOLDS FOR POWER-ON RESET (COMMERCIAL AND INDUSTRIAL)

Sophisticated power-up management circuitry is designed into every IGLOO nano device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1.

There are five regions to consider during power-up.

IGLOO nano I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 and Figure 2-2).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

2.1.2.1 VCCI Trip Point:

- Ramping up (V5 devices): 0.6V < trip_point_up < 1.2V
- Ramping down (V5 devices): 0.5V < trip_point_down < 1.1V
- Ramping up (V2 devices): 0.75V < trip_point_up < 1.05V
- Ramping down (V2 devices): 0.65V < trip_point_down < 0.95V

2.1.2.2 VCC Trip Point:

- Ramping up (V5 devices): 0.6V < trip_point_up < 1.1V
- Ramping down (V5 devices): 0.5V < trip_point_down < 1.0V
- Ramping up (V2 devices): 0.65V < trip_point_up < 1.05V
- Ramping down (V2 devices): 0.55V < trip_point_down < 0.95

VVCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

2.1.2.3 PLL Behavior at Brownout Condition

Microchip recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75V ± 0.25V for V5 devices, and 0.75V ± 0. V for V2 devices), the PLL output lock signal goes LOW and/or the output clock is lost. Refer to the "Brownout Voltage" section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for information on clock and lock recovery.

2.1.2.4 Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

FIGURE 2-1: V5 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS

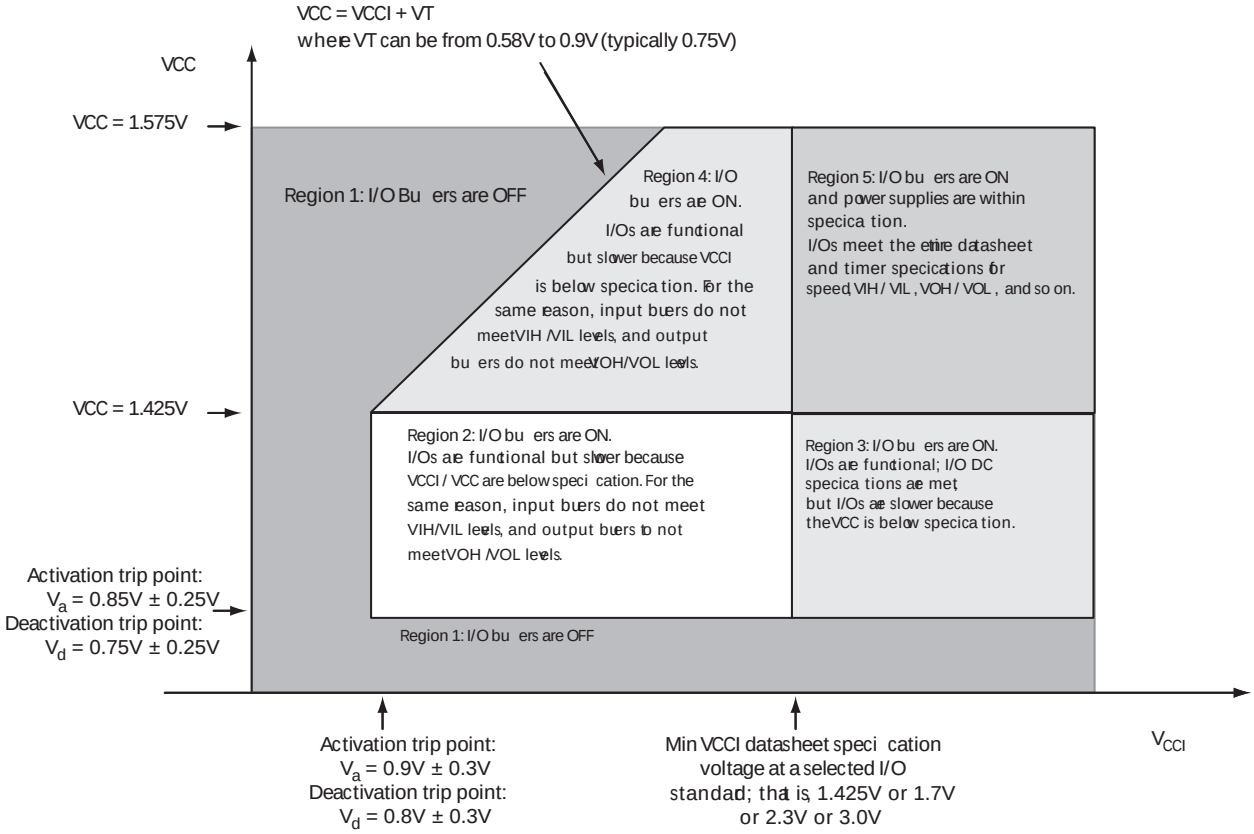
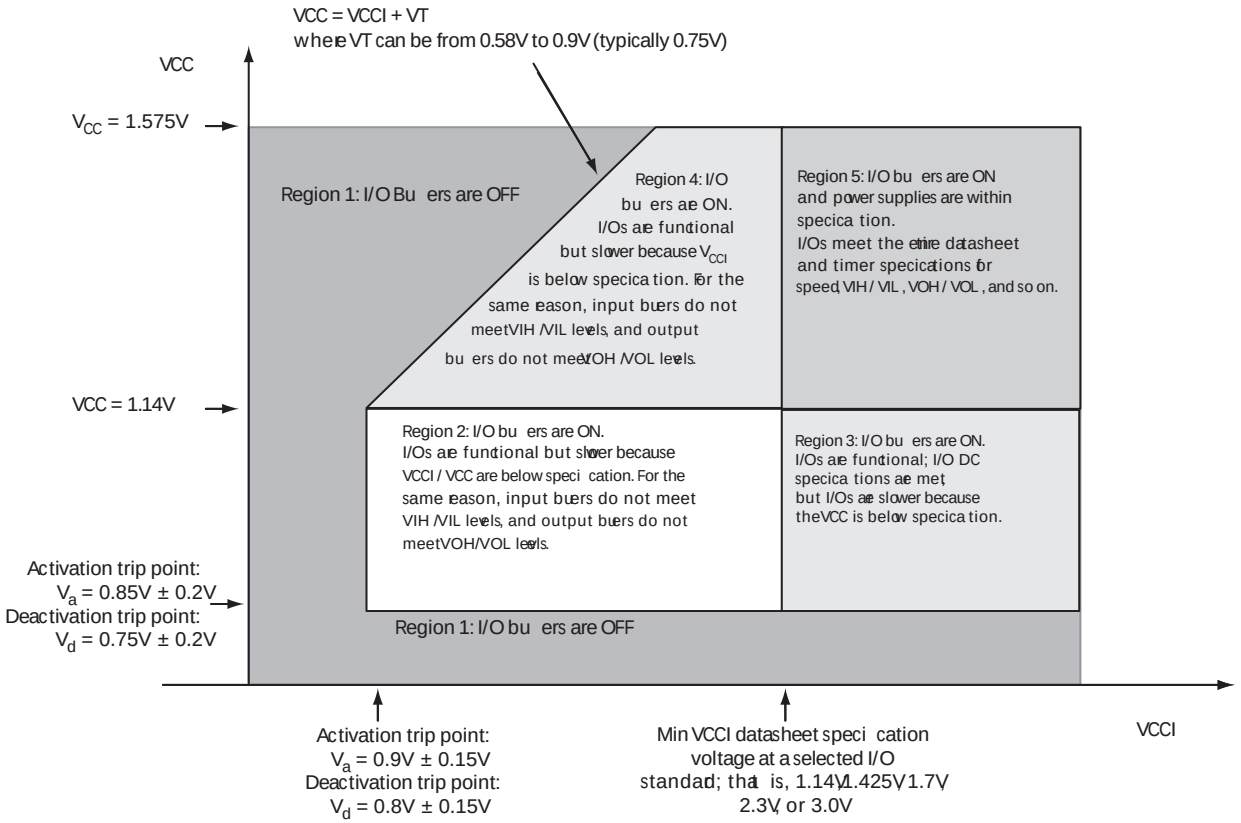


FIGURE 2-2: V2 DEVICES – I/O STATE AS A FUNCTION OF VCCI AND VCC VOLTAGE LEVELS



2.1.3 THERMAL CHARACTERISTICS

2.1.3.1 Introduction

The temperature variable in the Microchip Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

The following equation can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_A$

where:

T_A = Ambient temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Figure 2-5.

P = Power dissipation

2.1.3.2 Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The maximum operating junction temperature is 100 °C. The following equation shows a sample calculation of the maximum operating power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{100°C - 70°C}{20.5°C/W} = 1.46\ W$$

TABLE 2-5: PACKAGE THERMAL RESISTIVITIES

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	200 ft./ min.	500 ft./ min.	
Chip Scale Package (CSP)	36	TBD	TBD	TBD	TBD	C/W
	81	TBD	TBD	TBD	TBD	C/W
Quad Flat No Lead (QFN)	48	TBD	TBD	TBD	TBD	C/W
	68	TBD	TBD	TBD	TBD	C/W
	100	TBD	TBD	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)	100	10.0	35.3	29.4	27.1	C/W

2.1.3.3 Temperature and Voltage Derating Factors

The following table lists the temperature and voltage derating factors for timing delays at 1.5V DC core supply voltage.

TABLE 2-6: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO T_J = 70 °C, VCC = 1.425V) FOR IGLOO NANO V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE

Array Voltage VCC (V)	Junction Temperature (°C)						
	–40 °C	–20 °C	0 °C	25 °C	70 °C	85 °C	100 °C
1.425	0.947	0.956	0.965	0.978	1.000	1.009	1.013
1.5	0.875	0.883	0.892	0.904	0.925	0.932	0.937
1.575	0.821	0.829	0.837	0.848	0.868	0.875	0.879

The following table lists the temperature and voltage derating factors for timing delays at 1.2V DC core supply voltage.

TABLE 2-7: TEMPERATURE AND VOLTAGE DERATING FACTORS FOR TIMING DELAYS (NORMALIZED TO T_J = 70 °C, VCC = 1.14V) FOR IGLOO NANO V2, 1.2V DC CORE SUPPLY VOLTAGE

Array Voltage VCC (V)	Junction Temperature (°C)						
	–40 °C	–20 °C	0 °C	25 °C	70 °C	85 °C	100 °C
1.14	0.968	0.974	0.979	0.991	1.000	1.006	1.009
1.2	0.863	0.868	0.873	0.884	0.892	0.898	0.901
1.26	0.792	0.797	0.801	0.811	0.819	0.824	0.827

2.1.4 CALCULATING POWER DISSIPATION

2.1.4.1 Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power mode usage. Microchip recommends using the Power Calculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

The following table lists the power supply state per mode.

TABLE 2-8: POWER SUPPLY STATE PER MODE

Modes/Power Supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating

TABLE 2-8: POWER SUPPLY STATE PER MODE

Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power Supply level = 0V

The following table lists the quiescent supply current (IDD) characteristics for IGLOO nano Flash*Freeze mode.

TABLE 2-9: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO NANO FLASH*FREEZE MODE[1]

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25 °C)	1.2V	1.9	3.3	3.3	8	13	20	µA
	1.5V	5.8	6	6	10	18	34	µA

1. IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 through Table 2-14 and Table 2-15 through Table 2-18 (PDC6 and PDC7)

The following table lists the quiescent supply current (IDD) characteristics for IGLOO nano Sleep mode.

TABLE 2-10: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO NANO SLEEP MODE[1]

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
VCCI= 1.2V (per bank) Typical (25 °C)	1.2V	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI = 1.5V (per bank) Typical (25 °C)	1.2V/ 1.5V	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI = 1.8V (per bank) Typical (25 °C)	1.2V/ 1.5V	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI = 2.5V (per bank) Typical (25 °C)	1.2V/ 1.5V	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI = 3.3V (per bank) Typical (25 °C)	1.2V/ 1.5V	2.5	2.5	2.5	2.5	2.5	2.5	µA

1. $I_{DD} = N_{BANKS} * I_{CCI}$

The following table lists the quiescent supply current (IDD) characteristics for IGLOO nano Shutdown mode.

TABLE 2-11: QUIESCENT SUPPLY CURRENT (IDD) CHARACTERISTICS, IGLOO NANO SHUTDOWN MODE

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25 °C)	1.2V/1.5V	0	0	0	0	0	0	µA

The following table lists the quiescent supply current (IDD) characteristics for no IGLOO nano Flash*Freeze mode.

TABLE 2-12: QUIESCENT SUPPLY CURRENT (IDD), NO IGLOO NANO FLASH*FREEZE MODE[1]

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
ICCA Current[2]								

TABLE 2-12: QUIESCENT SUPPLY CURRENT (IDD), NO IGLOO NANO FLASH*FREEZE MODE[1]

	Core Voltage	AGLN010	AGLN015	AGLN020	AGLN060	AGLN125	AGLN250	Units
Typical (25 °C)	1.2V	3.7	5	5	10	13	18	µA
	1.5V	8	14	14	20	28	44	µA
ICCI or IJTAG Current								
VCCI/VJTAG = 1.2V (per bank) Typical (25 °C)	1.2V	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5V (per bank) Typical (25 °C)	1.2V/1.5V	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8V (per bank) Typical (25 °C)	1.2V/1.5V	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI/VJTAG = 2.5V (per bank) Typical (25 °C)	1.2V/1.5V	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3V (per bank) Typical (25 °C)	1.2V/1.5V	2.5	2.5	2.5	2.5	2.5	2.5	µA

Note 1: IDD = N_{BANKS} * ICCI + ICCA. JTAG counts as one bank when powered.

2: Includes VCC, VCCPLL, and VPUMP currents.

2.1.4.2 Power per I/O Pin

The following table lists the summary of I/O input buffer power (per pin) at the default I/O software settings applicable to IGLOO nano I/O banks.

TABLE 2-13: SUMMARY OF I/O INPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS APPLICABLE TO IGLOO NANO I/O BANKS

	VCCI (V)	Dynamic Power PAC9 (µW/MHz) [1]
Single-Ended		
3.3V LVTTL/3.3V LVCMOS	3.3	16.38
3.3V LVTTL/3.3V LVCMOS – Schmitt Trigger	3.3	18.89
3.3V LVCMOS Wide Range[2]	3.3	16.38
3.3V LVCMOS Wide Range – Schmitt Trigger	3.3	18.89
2.5V LVCMOS	2.5	4.71
2.5V LVCMOS – Schmitt Trigger	2.5	6.13
1.8V LVCMOS	1.8	1.64
1.8V LVCMOS – Schmitt Trigger	1.8	1.79
1.5V LVCMOS (JESD8-11)	1.5	0.97
1.5V LVCMOS (JESD8-11) – Schmitt Trigger	1.5	0.96
1.2V LVCMOS[3]	1.2	0.57
1.2V LVCMOS – Schmitt Trigger[3]	1.2	0.52
1.2V LVCMOS Wide Range[3]	1.2	0.57
1.2V LVCMOS Wide Range – Schmitt Trigger[3]	1.2	0.52

Note 1: PAC9 is the total dynamic power measured on V_{CCI}.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

3: Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.

The following table lists the summary of I/O output buffer power (per pin) at the default I/O software settings applicable to IGLOO nano I/O banks.

TABLE 2-14: SUMMARY OF I/O OUTPUT BUFFER POWER (PER PIN) – DEFAULT I/O SOFTWARE SETTINGS[1] APPLICABLE TO IGLOO NANO I/O BANKS

	C_{LOAD} (pF)	VCCI (V)	Dynamic Power PAC10 (µW/MHz)[2]
Single-Ended			
3.3V LVTTL/3.3V LVCMOS	5	3.3	107.98
3.3V LVCMOS Wide Range[3]	5	3.3	107.98
2.5V LVCMOS	5	2.5	61.24
1.8V LVCMOS	5	1.8	31.28
1.5V LVCMOS (JESD8-11)	5	1.5	21.50
1.2V LVCMOS[4]	5	1.2	15.22

Note 1: Dynamic power consumption is given for standard load and software default drive strength and output slew.

2: PAC10 is the total dynamic power measured on VCCI.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range as specified in the JESD8-B specification.

4: Applicable for IGLOO nano V2 devices operating at VCCI ≥ VCC.

2.1.4.3 Power Consumption of Various Internal Resources

The following table lists the different components contributing to the dynamic power consumption in IGLOO nano devices for IGLOO nano V2 or V5 devices at 1.5V core voltage.

TABLE 2-15: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO NANO DEVICES FOR IGLOO NANO V2 OR V5 DEVICES, 1.5V CORE SUPPLY VOLTAGE

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	4.421	4.493	2.700	0	0	0
PAC2	Clock contribution of a Global Spine	2.704	1.976	1.982	4.002	4.002	2.633
PAC3	Clock contribution of a VersaTile row	1.496	1.504	1.511	1.346	1.346	1.340
PAC4	Clock contribution of a VersaTile used as a sequential module	0.152	0.153	0.153	0.148	0.148	0.143
PAC5	First contribution of a VersaTile used as a sequential module	0.057					
PAC6	Second contribution of a VersaTile used as a sequential module	0.207					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.17					
PAC8	Average contribution of a routing net	0.7					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13.					

TABLE 2-15: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO NANO DEVICES FOR IGLOO NANO V2 OR V5 DEVICES, 1.5V CORE SUPPLY VOLTAGE

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14.					
PAC11	Average contribution of a RAM block during a read operation	25.00			—		
PAC12	Average contribution of a RAM block during a write operation	30.00			—		
PAC13	Dynamic contribution for PLL	2.70			—		

The following table lists the different components contributing to the static power consumption in IGLOO nano devices for IGLOO nano V2 or V5 devices at 1.5V core voltage.

TABLE 2-16: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN IGLOO NANO DEVICES FOR IGLOO NANO V2 OR V5 DEVICES, 1.5V CORE SUPPLY VOLTAGE

Parameter	Definition	Device -Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12					
PDC2	Array static power in Static (Idle) mode	See Table 2-12					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9					
PDC4 [1]	Static PLL contribution	1.84			—		
PDC5	Bank quiescent power (VCCI-dependent)[2]	See Table 2-12					

Note 1: Minimum contribution of the PLL when running at lowest frequency.

2: For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or the SmartPower tool in Libero SoC.

The following table lists the different components contributing to the dynamic power consumption in IGLOO nano devices for IGLOO nano V2 devices at 1.2V core voltage.

TABLE 2-17: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO NANO DEVICES FOR IGLOO NANO V2 DEVICES, 1.2V CORE SUPPLY VOLTAGE

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC1	Clock contribution of a Global Rib	2.829	2.875	1.728	0	0	0
PAC2	Clock contribution of a Global Spine	1.731	1.265	1.268	2.562	2.562	1.685
PAC3	Clock contribution of a VersaTile row	0.957	0.963	0.967	0.862	0.862	0.858

TABLE 2-17: DIFFERENT COMPONENTS CONTRIBUTING TO DYNAMIC POWER CONSUMPTION IN IGLOO NANO DEVICES FOR IGLOO NANO V2 DEVICES, 1.2V CORE SUPPLY VOLTAGE

Parameter	Definition	Device-Specific Dynamic Power (µW/MHz)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PAC4	Clock contribution of a VersaTile used as a sequential module	0.098	0.098	0.098	0.094	0.094	0.091
PAC5	First contribution of a VersaTile used as a sequential module	0.045					
PAC6	Second contribution of a VersaTile used as a sequential module	0.186					
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11					
PAC8	Average contribution of a routing net	0.45					
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13					
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-14					
PAC11	Average contribution of a RAM block during a read operation	25.00			—		
PAC12	Average contribution of a RAM block during a write operation	30.00			—		
PAC13	Dynamic contribution for PLL	2.10			—		

The following table lists the different components contributing to the static power consumption in IGLOO nano devices for IGLOO nano V2 devices at 1.2V core voltage.

TABLE 2-18: DIFFERENT COMPONENTS CONTRIBUTING TO THE STATIC POWER CONSUMPTION IN IGLOO NANO DEVICES FOR IGLOO NANO V2 DEVICES, 1.2V CORE SUPPLY VOLTAGE

Parameter	Definition	Device-Specific Static Power (mW)					
		AGLN250	AGLN125	AGLN060	AGLN020	AGLN015	AGLN010
PDC1	Array static power in Active mode	See Table 2-12					
PDC2	Array static power in Static (Idle) mode	See Table 2-12					
PDC3	Array static power in Flash*Freeze mode	See Table 2-9					
PDC4 [1]	Static PLL contribution	0.90			—		
PDC5	Bank quiescent power (VCCI-dependent)[2]	See Table 2-12					

Note 1: Minimum contribution of the PLL when running at lowest frequency.

2: For a different output load, drive strength, or slew rate, Microchip recommends using the Microchip power spreadsheet calculator or the SmartPower tool in Libero SoC.

2.1.4.4 Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated

- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-20.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-20. The calculation should be repeated for each clock domain defined in the design.

2.1.4.4.1 Total Power Consumption—P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

2.1.4.4.2 Total Static Power Consumption—P_{STAT}

$$P_{STAT} = (PDC1 \text{ or } PDC2 \text{ or } PDC3) + N_{BANKS} * PDC5$$

N_{BANKS} is the number of I/O banks powered in the design.

2.1.4.4.3 Total Dynamic Power Consumption—P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

2.1.4.4.4 Global Clock Contribution—P_{CLOCK}

$$P_{CLOCK} = (PAC1 + N_{SPINE} * PAC2 + N_{ROW} * PAC3 + N_{S\text{-}CELL} * PAC4) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO nano FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

PAC1, PAC2, PAC3, and PAC4 are device-dependent.

2.1.4.4.5 Sequential Cells Contribution—$P_{S\text{-}CELL}$

$$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (PAC5 + \alpha_1 / 2 * PAC6) * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19.

F_{CLK} is the global clock signal frequency.

2.1.4.4.6 Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * PAC7 * F_{CLK}$$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19.

F_{CLK} is the global clock signal frequency.

2.1.4.4.7 Routing Net Contribution—P_{NET}

$$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * PAC8 * F_{CLK}$$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-19.

F_{CLK} is the global clock signal frequency.

2.1.4.4.8 I/O Input Buffer Contribution—P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * PAC9 * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19.

F_{CLK} is the global clock signal frequency.

2.1.4.4.9 I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * PAC10 * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-20.

F_{CLK} is the global clock signal frequency.

2.1.4.4.10 RAM Contribution—P_{MEMORY}

$P_{MEMORY} = PAC11 * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + PAC12 * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-20.

2.1.4.4.11 PLL Contribution—P_{PLL}

$P_{PLL} = PDC4 + PAC13 * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.†

2.1.4.5 Guidelines

2.1.4.5.1 Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

2.1.4.5.2 Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

TABLE 2-19: TOGGLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

†. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution (PAC13 FCLKOUT product) to the total PLL contribution.*

TABLE 2-20: ENABLE RATE GUIDELINES RECOMMENDED FOR POWER CALCULATION

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

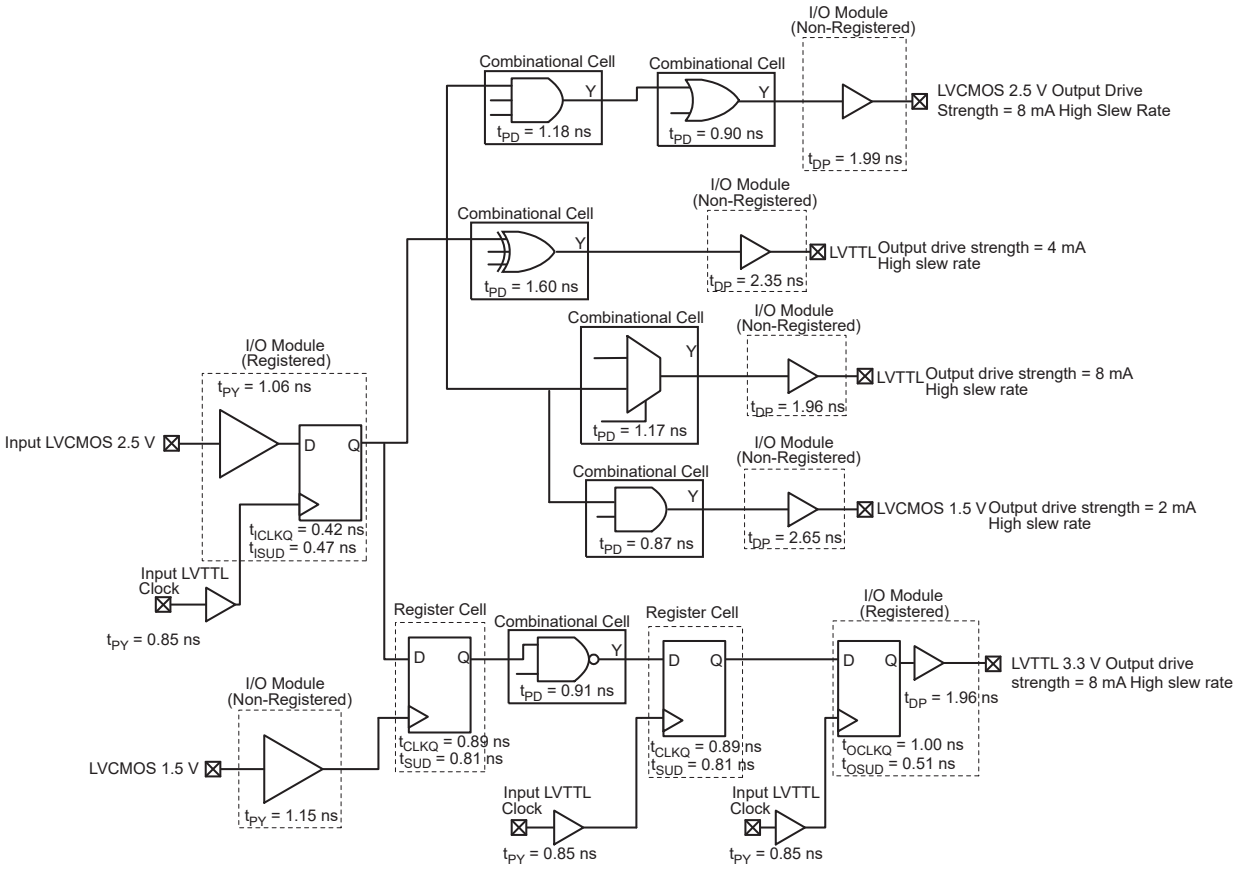
2.2 User I/O Characteristics

This section discusses the user I/O characteristics.

2.2.1 TIMING MODEL

The following figure shows the timing model operating conditions for the V2 and V5 devices.

FIGURE 2-3: TIMING MODEL OPERATING CONDITIONS: STD SPEED, COMMERCIAL TEMPERATURE RANGE (TJ = 70 °C), WORST-CASE VCC = 1.425V, FOR DC 1.5V CORE VOLTAGE, APPLICABLE TO V2 AND V5 DEVICES



The following figures show the timing model and delays for the input, output, and tristate Output buffer of the V2 and V5 devices.

FIGURE 2-4: INPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)

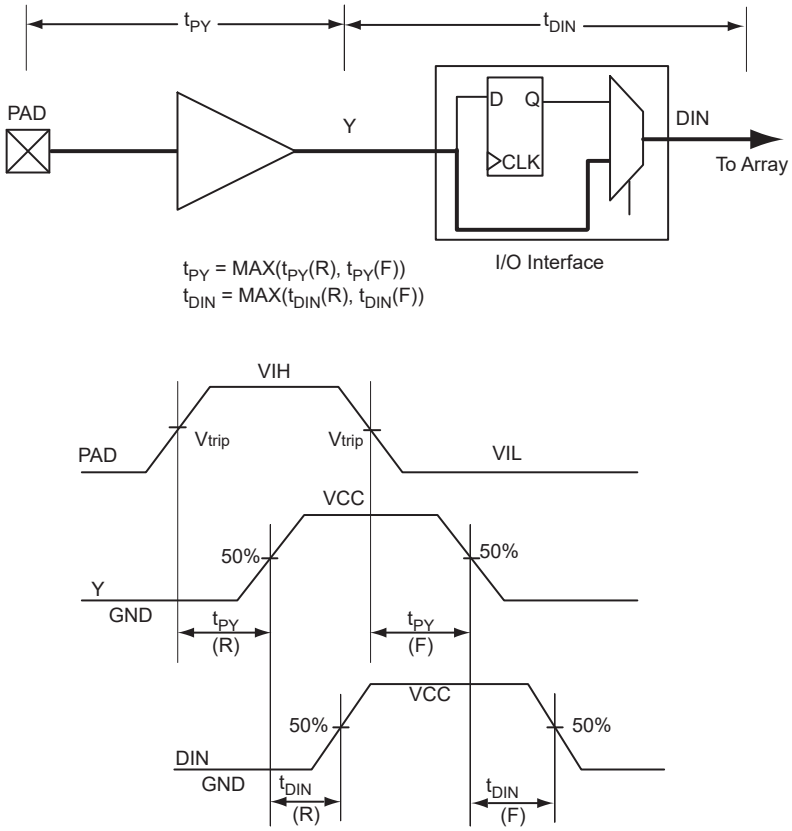


FIGURE 2-5: OUTPUT BUFFER MODEL AND DELAYS (EXAMPLE)

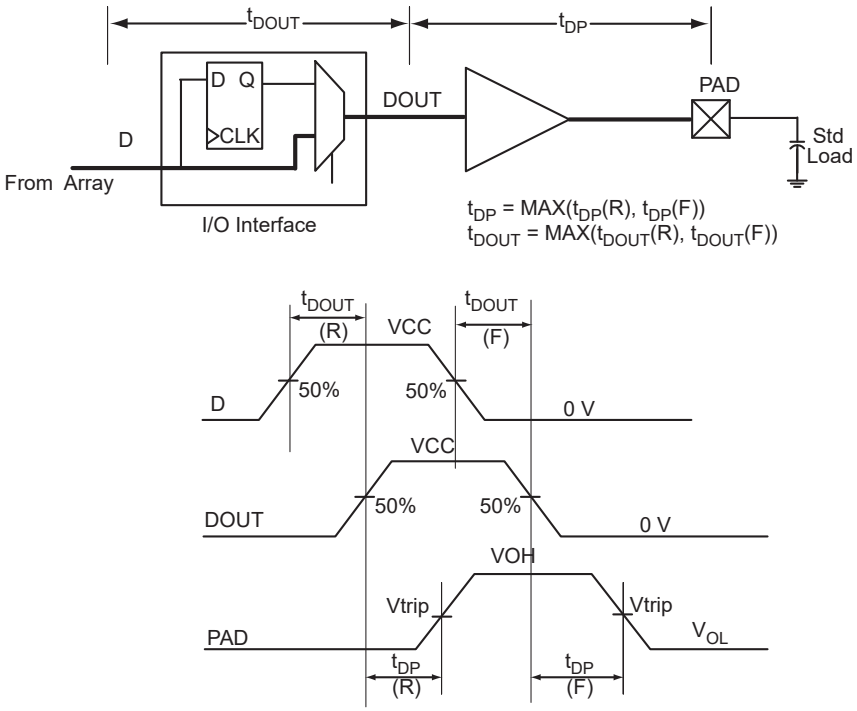
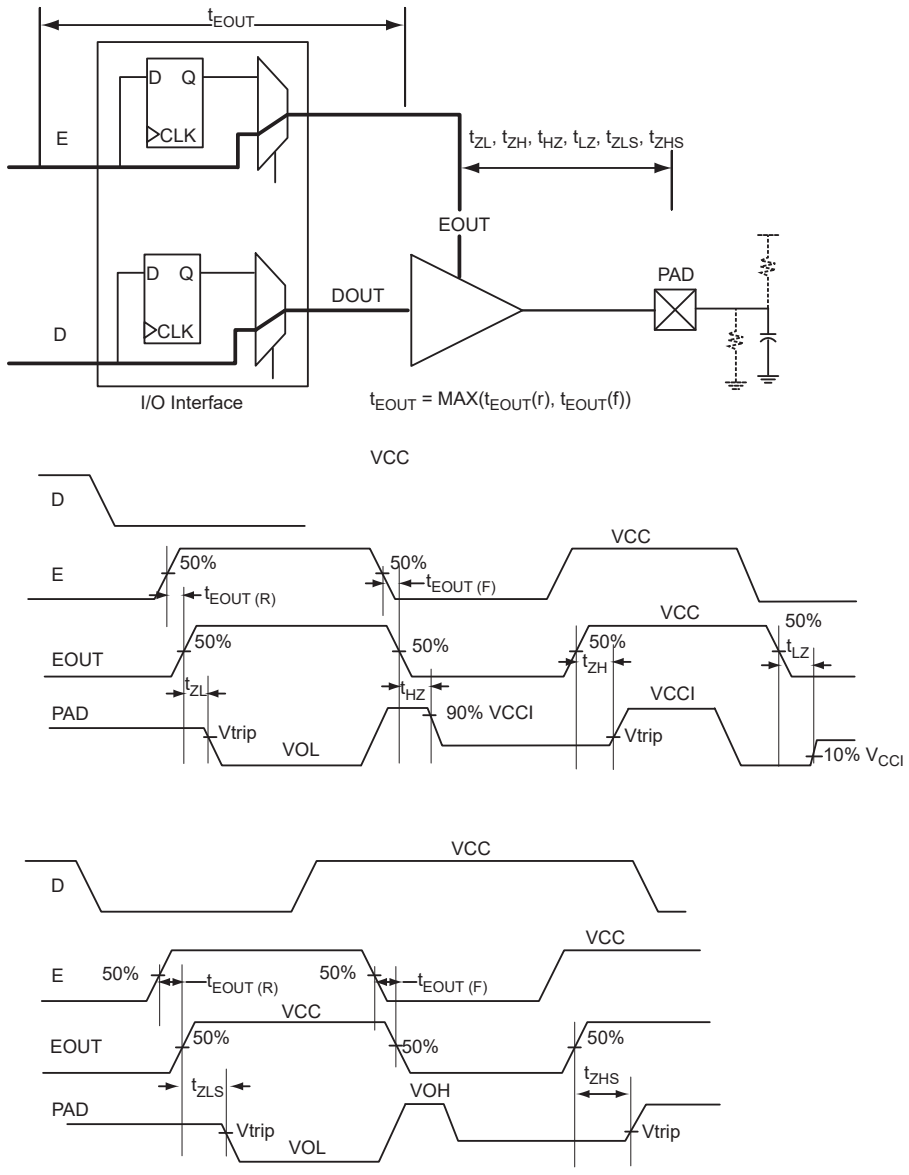


FIGURE 2-6: TRISTATE OUTPUT BUFFER TIMING MODEL AND DELAYS (EXAMPLE)



2.3 Overview of I/O Performance

2.3.1 SUMMARY OF I/O DC INPUT AND OUTPUT LEVELS – DEFAULT I/O SOFTWARE SETTINGS

The following table lists the summary of the maximum and minimum DC input levels applicable to commercial and industrial conditions at software default settings.

TABLE 2-21: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT AND OUTPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS—SOFTWARE DEFAULT SETTINGS

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1]	IOH[1]
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3V LVTTL / 3.3V LVCMOS	8 mA	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
3.3V LVCMOS Wide Range[3]	100 µA	8 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100 µA	100 µA
2.5V LVCMOS	8 mA	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5V LVCMOS	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2V LVCMOS[4]	1 mA	1 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1
1.2V LVCMOS Wide Range[4,5]	100 µA	1 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	100 µA	100 µA

Note 1: Currents are measured at 85 °C junction temperature.

2: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

3: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range, as specified in the JESD8-B specification.

4: Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.

5: All LVCMOS 1.2V software macros support LVCMOS 1.2V wide range, as specified in the JESD8-12 specification.

The following table lists the summary of the maximum and minimum DC input levels applicable to commercial and industrial conditions.

TABLE 2-22: SUMMARY OF MAXIMUM AND MINIMUM DC INPUT LEVELS APPLICABLE TO COMMERCIAL AND INDUSTRIAL CONDITIONS

DC I/O Standards	Commercial[1]		Industrial[2]	
	IIL [3]	IIH [4]	IIL [3]	IIH [4]
	µA	µA	µA	µA
3.3V LVTTL/3.3V LVCMOS	10	10	15	15
3.3V LVCOMS Wide Range	10	10	15	15
2.5V LVCMOS	10	10	15	15
1.8V LVCMOS	10	10	15	15
1.5V LVCMOS	10	10	15	15
1.2V LVCMOS[5]	10	10	15	15
1.2V LVCMOS Wide Range[5]	10	10	15	15

Note 1: Commercial range (–20 °C < T_A < 70 °C)

2: Industrial range (–40 °C < T_A < 85 °C)

3: I_{IH} is the input leakage current per I/O pin over recommended operating conditions, where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

4: I_{IL} is the input leakage current per I/O pin over recommended operating conditions, where –0.3V < VIN < VIL.

5: Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.

2.3.2 SUMMARY OF I/O TIMING CHARACTERISTICS – DEFAULT I/O SOFTWARE SETTINGS

The following table lists the summary of the AC measuring points.

TABLE 2-23: SUMMARY OF AC MEASURING POINTS

Standard	Measuring Trip Point (Vtrip)
3.3V LVTTL/3.3V LVCMOS	1.4V
3.3V LVCMOS Wide Range	1.4V
2.5V LVCMOS	1.2V
1.8V LVCMOS	0.90V
1.5V LVCMOS	0.75V
1.2V LVCMOS	0.60V
1.2V LVCMOS Wide Range	0.60V

The following table lists the summary of the I/O AC parameter definitions.

TABLE 2-24: I/O AC PARAMETER DEFINITIONS

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z

TABLE 2-24: I/O AC PARAMETER DEFINITIONS

Parameter	Parameter Definition
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

2.3.2.1 Applies to IGLOO nano at 1.5V Core Operating Conditions

The following table lists the summary of I/O timing characteristics of IGLOO nano at 1.5V core operating conditions.

TABLE 2-25: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS STD SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V

I/O Standard	Drive Strength (mA)	Equivalent Software Default t Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3V LVTTL / 3.3V LVCMOS	8 mA	8 mA	High	5 pF	0.97	1.79	0.19	0.86	1.16	0.66	1.83	1.45	1.98	2.38	ns
3.3 V LVCMOS Wide Range[2]	100 µA	8 mA	High	5 pF	0.97	2.56	0.19	1.20	1.66	0.66	2.57	2.02	2.82	3.31	ns
2.5V LVCMOS	8 mA	8 mA	High	5 pF	0.97	1.81	0.19	1.10	1.24	0.66	1.85	1.63	1.97	2.26	ns
1.8V LVCMOS	4 mA	4 mA	High	5 pF	0.97	2.08	0.19	1.03	1.44	0.66	2.12	1.95	1.99	2.19	ns
1.5V LVCMOS	2 mA	2 mA	High	5 pF	0.97	2.39	0.19	1.19	1.52	0.66	2.44	2.24	2.02	2.15	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range, as specified in the JESD8-B specification.

3: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.2.2 Applies to IGLOO nano at 1.2V Core Operating Conditions

The following table lists the summary of I/O timing characteristics of IGLOO nano at 1.2V core operating conditions.

TABLE 2-26: SUMMARY OF I/O TIMING CHARACTERISTICS—SOFTWARE DEFAULT SETTINGS STD SPEED GRADE, COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 3.0V

I/O Standard	Drive Strength (mA)	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY})	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
3.3V LVTTL / 3.3V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
3.3 V LVCMOS Wide Range[2]	100 µA	8 mA	High	5 pF	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
2.5V LVCMOS	8 mA	8 mA	High	5 pF	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
1.8V LVCMOS	4 mA	4 mA	High	5 pF	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns
1.5V LVCMOS	2 mA	2 mA	High	5 pF	1.55	2.78	0.26	1.27	1.77	1.10	2.82	2.62	2.44	2.74	ns
1.2V LVCMOS	1 mA	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns
1.2 V LVCMOS Wide Range[3]	100 µA	1 mA	High	5 pF	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

Note 1: The minimum drive strength for any LVCMOS 1.2V or LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range, as specified in the JESD8-B specification.

3: All LVCMOS 1.2V software macros support LVCMOS 1.2V side range as specified in the JESD8-12 specification.

4: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.3 DETAILED I/O DC CHARACTERISTICS

TABLE 2-27: INPUT CAPACITANCE

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

The following table lists the I/O output buffer maximum resistances.

TABLE 2-28: I/O OUTPUT BUFFER MAXIMUM RESISTANCES [1]

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3V LVTTL/3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	

TABLE 2-28: I/O OUTPUT BUFFER MAXIMUM RESISTANCES [1]

2.5V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5V LVCMOS	2 mA	200	224
1.2V LVCMOS [4]	1 mA	315	315
1.2V LVCMOS Wide Range [4]	100 µA	315	315

Note 1: These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models posted at https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas#ibis.

2: $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec

3: $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / I_{OHspec}

4: Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.

The following table lists the I/O weak pull-up/pull-down resistances minimum and maximum resistance Values.

TABLE 2-29: I/O WEAK PULL-UP/PULL-DOWN RESISTANCES (MINIMUM AND MAXIMUM WEAK PULL-UP/PULL-DOWN RESISTANCE VALUES)

VCCI	$R_{(WEAK\ PULL\text{-}UP)}$ [1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$ [2] (Ω)	
	Min.	Max.	Min.	Max.
3.3V	10KK	45K	10K	45K
3.3V (wide range I/Os)	10K	45K	10K	45K
2.5V	11K	55K	12K	74K
1.8V	18K	70K	17K	110K
1.5V	19K	90K	19K	140K
1.2V	25K	110K	25K	150K
1.2V (wide range I/Os)	19K	110K	19K	150K

Note 1: $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / $I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

2: $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / $I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

The following table lists the I/O short currents IOSH/IOSL.

TABLE 2-30: I/O SHORT CURRENTS IOSH/IOSL

	Drive Strength	IOSL (mA)[1]	IOSH (mA)*
3.3V LVTTL/3.3V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
3.3V LVCMOS Wide Range	100 µA	Same as equivalent software default drive	
2.5V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8V LVCMOS	2 mA	9	11
	4 mA	17	22

TABLE 2-30: I/O SHORT CURRENTS IOSH/IOSL

	Drive Strength	IOSL (mA)[1]	IOSH (mA)*
1.5V LVCMOS	2 mA	13	16
1.2V LVCMOS	1 mA	10	13
1.2V LVCMOS Wide Range	100 µA	10	13

1. T_J = 100 °C

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3V, 8 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100 °C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

The following table lists the duration I/O can withstand IOSH/IOSL events depending on the junction temperature.

TABLE 2-31: DURATION OF SHORT CIRCUIT EVENT BEFORE FAILURE

Temperature	Time before Failure
–40 °C	> 20 years
–20 °C	> 20 years
0 °C	> 20 years
25 °C	> 20 years
70 °C	5 years
85 °C	2 years
100 °C	6 months

The following table lists the hysteresis voltage value (Typ.) for the Schmitt mode input buffers.

TABLE 2-32: SCHMITT TRIGGER INPUT HYSTERESIS (HYSTERESIS VOLTAGE VALUE (TYP.) FOR SCHMITT MODE INPUT BUFFERS)

Input Buffer Configuration	Hysteresis Value (typ.)
3.3V LVTTL/LVCMOS (Schmitt trigger mode)	240 mV
2.5V LVCMOS (Schmitt trigger mode)	140 mV
1.8V LVCMOS (Schmitt trigger mode)	80 mV
1.5V LVCMOS (Schmitt trigger mode)	60 mV
1.2V LVCMOS (Schmitt trigger mode)	40 mV

The following table lists the I/O input rise time, fall time, and related I/O reliability.

TABLE 2-33: I/O INPUT RISE TIME, FALL TIME, AND RELATED I/O RELIABILITY

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS (Schmitt trigger disabled)	No requirement	10 ns [1]	20 years (100 °C)
LVTTL/LVCMOS (Schmitt trigger enabled)	No requirement	No requirement, but input noise voltage cannot exceed Schmitt hysteresis.	20 years (100 °C)

1. The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microchip recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

2.3.4 SINGLE-ENDED I/O CHARACTERISTICS

The following sections discuss single-ended I/O characteristics.

2.3.4.1 3.3V LVTTL/LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

TABLE 2-34: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

3.3V LVTTL/ 3.3V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA [4]	µA [4]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Note 1: I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

2: I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

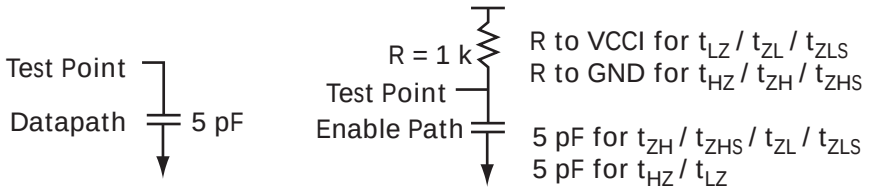
3: Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

4: Currents are measured at 85 °C junction temperature.

5: Software default selection highlighted in gray.

The following figure shows the AC loading of 3.3V LVTTL/LVCMOS .

FIGURE 2-7: AC LOADING



The following table lists the 3.3V LVTTL/LVCMOS AC waveforms, measuring Points, and capacitive loads.

TABLE 2-35: 3.3V LVTTL/LVCMOS AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input LOW (V)	Input HIGH (V)	Measuring Point[1] (V)	C_{LOAD} (pF)
0	3.3	1.4	5

1. Measuring point = Vtrip. For a complete table of trip points, seeTable 2-23.

2.3.4.1.1 Timing Characteristics: Applies to 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the 3.3V LVTTL/3.3V LVCMOS low slew commercial-case conditions.

TABLE 2-36: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 3.0V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	3.52	0.19	0.86	1.16	0.66	3.59	3.42	1.75	1.90	ns
4 mA	STD	0.97	3.52	0.19	0.86	1.16	0.66	3.59	3.42	1.75	1.90	ns
6 mA	STD	0.97	2.90	0.19	0.86	1.16	0.66	2.96	2.83	1.98	2.29	ns
8 mA	STD	0.97	2.90	0.19	0.86	1.16	0.66	2.96	2.83	1.98	2.29	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.5V DC core voltage for the 3.3V LVTTL/3.3V LVCMOS high slew commercial-case conditions.

TABLE 2-37: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 3.0V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.16	0.19	0.86	1.16	0.66	2.20	1.80	1.75	1.99	ns
4 mA	STD	0.97	2.16	0.19	0.86	1.16	0.66	2.20	1.80	1.75	1.99	ns
6 mA	STD	0.97	1.79	0.19	0.86	1.16	0.66	1.83	1.45	1.98	2.38	ns
8 mA	STD	0.97	1.79	0.19	0.86	1.16	0.66	1.83	1.45	1.98	2.38	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.1.2 Timing Characteristics: Applies to 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the 3.3V LVTTL/3.3V LVCMOS low slew commercial-case conditions.

TABLE 2-38: 3.3V LVTTL/3.3V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 3.0V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
4 mA	STD	1.55	4.09	0.26	0.97	1.36	1.10	4.16	3.91	2.19	2.64	ns
6 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns
8 mA	STD	1.55	3.45	0.26	0.97	1.36	1.10	3.51	3.32	2.43	3.03	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the 3.3V LVTTL/3.3V LVCMOS high slew commercial-case conditions.

TABLE 2-39: 3.3V LVTTL/3.3V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 3.0V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
4 mA	STD	1.55	2.68	0.26	0.97	1.36	1.10	2.72	2.26	2.19	2.74	ns
6 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns
8 mA	STD	1.55	2.31	0.26	0.97	1.36	1.10	2.34	1.90	2.43	3.14	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.2 3.3V LVCMOS Wide Range

The following table lists the minimum and maximum DC input and output levels for LVCMOS 3.3V wide range.

TABLE 2-40: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS FOR LVCMOS 3.3V WIDE RANGE

3.3V LVCMOS Wide Range[1]	Equivalent Software Default Drive Strength Option[4]	VIL		VIH		VOL	VOH	IOL	I_{OH}	IIL [2]	IIH [3]
Drive Strength		Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	100	100	10	10

Note 1: All LVCMOS 3.3V software macros support LVCMOS 3.3V Wide Range, as specified in the JEDEC JESD8-B specification.

2: I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

3: I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

4: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

5: Currents are measured at 85 °C junction temperature.

6: Software default selection is highlighted in gray.

2.3.4.2.1 Timing Characteristics: Applies to 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the 3.3V LVCMOS slow slew commercial-case conditions.

TABLE 2-41: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.97	5.23	0.19	1.20	1.66	0.66	5.24	5.00	2.47	2.56	ns
100 µA	4 mA	STD	0.97	5.23	0.19	1.20	1.66	0.66	5.24	5.00	2.47	2.56	ns
100 µA	6 mA	STD	0.97	4.27	0.19	1.20	1.66	0.66	4.28	4.12	2.83	3.16	ns
100 µA	8 mA	STD	0.97	4.27	0.19	1.20	1.66	0.66	4.28	4.12	2.83	3.16	ns

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.5V DC core voltage for the 3.3V LVCMOS high slew commercial-case conditions.

TABLE 2-42: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.425V, Worst-Case VCCI = 2.7 V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	0.97	3.11	0.19	1.20	1.66	0.66	3.13	2.55	2.47	2.70	ns
100 µA	4 mA	STD	0.97	3.11	0.19	1.20	1.66	0.66	3.13	2.55	2.47	2.70	ns
100 µA	6 mA	STD	0.97	2.56	0.19	1.20	1.66	0.66	2.57	2.02	2.82	3.31	ns
100 µA	8 mA	STD	0.97	2.56	0.19	1.20	1.66	0.66	2.57	2.02	2.82	3.31	ns

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

3: Software default selection highlighted in gray.

2.3.4.2.2 Timing Characteristics: Applies to 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the 3.3V LVCMOS low slew commercial-case conditions.

TABLE 2-43: 3.3V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 µA	4 mA	STD	1.55	6.01	0.26	1.31	1.91	1.10	6.01	5.66	3.02	3.49	ns
100 µA	6 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns
100 µA	8 mA	STD	1.55	5.02	0.26	1.31	1.91	1.10	5.02	4.76	3.38	4.10	ns

Note 1: The minimum drive strength for any LVCMOS 3.3V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the 3.3V LVCMOS high slew commercial-case conditions.

TABLE 2-44: 3.3V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE

Commercial-Case Conditions: T_J = 70 °C, Worst-Case VCC = 1.14V, Worst-Case VCCI = 2.7V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 µA	4 mA	STD	1.55	3.82	0.26	1.31	1.91	1.10	3.82	3.15	3.01	3.65	ns
100 µA	6 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns
100 µA	8 mA	STD	1.55	3.25	0.26	1.31	1.91	1.10	3.25	2.61	3.38	4.27	ns

Note 1: The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

3: Software default selection highlighted in gray.

2.3.4.3 2.5V LVCMOS

Low-Voltage CMOS for 2.5V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5V applications.

TABLE 2-45: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

2.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL 1	IIH 2
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[3]	Max., mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10

TABLE 2-45: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

2.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[3]	Max., mA[3]	µA[4]	µA[4]
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Note 1: I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

2: I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

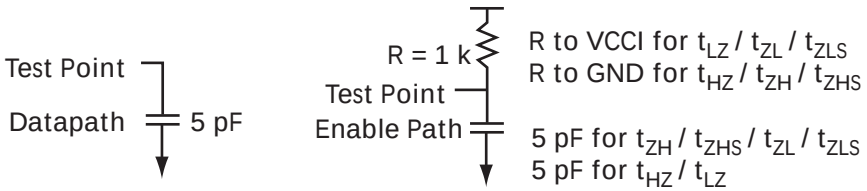
3: Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

4: Currents are measured at 85 °C junction temperature.

5: Software default selection highlighted in gray.

The following figure shows the AC loading of 2.5V LVCMOS.

FIGURE 2-8: AC LOADING



The following table lists the 2.5V LVCMOS AC waveforms, measuring points, and capacitive loads.

TABLE 2-46: 2.5V LVCMOS AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input LOW (V)	Input HIGH (V)	Measuring Point[1] (V)	C_{LOAD} (pF)
0	2.5	1.2	5

1. Measuring point = Vtrip. For a complete table of trip points, see Table 2-23.

2.3.4.3.1 Timing Characteristics: Applies to 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the 2.5V LVCMOS low slew commercial-case conditions.

TABLE 2-47: 2.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.3V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	4.13	0.19	1.10	1.24	0.66	4.01	4.13	1.73	1.74	ns
4 mA	STD	0.97	4.13	0.19	1.10	1.24	0.66	4.01	4.13	1.73	1.74	ns
8 mA	STD	0.97	3.39	0.19	1.10	1.24	0.66	3.31	3.39	1.98	2.19	ns
8 mA	STD	0.97	3.39	0.19	1.10	1.24	0.66	3.31	3.39	1.98	2.19	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.5V DC core voltage for the 2.5V LVCMOS high slew commercial-case conditions.

TABLE 2-48: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 2.3V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.19	0.19	1.10	1.24	0.66	2.23	2.11	1.72	1.80	ns
4 mA	STD	0.97	2.19	0.19	1.10	1.24	0.66	2.23	2.11	1.72	1.80	ns
6 mA	STD	0.97	1.81	0.19	1.10	1.24	0.66	1.85	1.63	1.97	2.26	ns
8 mA	STD	0.97	1.81	0.19	1.10	1.24	0.66	1.85	1.63	1.97	2.26	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.3.2 Timing Characteristics: Applies to 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the 2.5V LVCMOS low slew commercial-case conditions.

TABLE 2-49: 2.5 LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 2.3V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
4 mA	STD	1.55	4.61	0.26	1.21	1.39	1.10	4.55	4.61	2.15	2.43	ns
6 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns
8 mA	STD	1.55	3.86	0.26	1.21	1.39	1.10	3.82	3.86	2.41	2.89	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the 2.5V LVCMOS high slew commercial-case conditions.

TABLE 2-50: 2.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 2.3V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
4 mA	STD	1.55	2.68	0.26	1.21	1.39	1.10	2.72	2.54	2.15	2.51	ns
6 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns
8 mA	STD	1.55	2.30	0.26	1.21	1.39	1.10	2.33	2.04	2.41	2.99	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.4 1.8V LVCMOS

Low-voltage CMOS for 1.8V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8V applications. It uses a 1.8V input buffer and a push-pull output buffer.

TABLE 2-51: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

1.8V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	I_{IL}[1]	I_{IH}[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Note 1: I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

2: I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

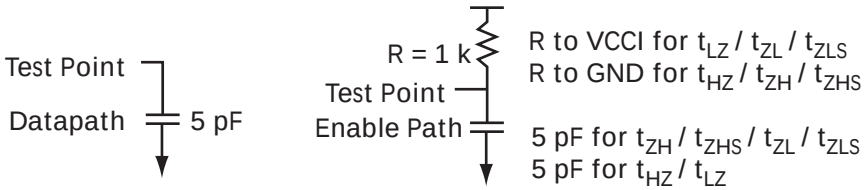
3: Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

4: Currents are measured at 85 °C junction temperature.

5: Software default selection highlighted in gray.

The following figure shows the AC loading of 1.8V LVCMOS.

FIGURE 2-9: AC LOADING



The following table lists the 1.8V LVCMOS AC waveforms, measuring Points, and capacitive loads.

TABLE 2-52: 1.8V LVCMOS AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input LOW (V)	Input HIGH (V)	Measuring Point[1] (V)	C_{LOAD} (pF)
0	1.8	0.9	5

1. Measuring point = Vtrip. For a complete table of trip points, see Table 2-23.

2.3.4.4.1 Timing Characteristics: Applies to 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the 1.8V LVCMOS low slew commercial-case conditions.

TABLE 2-53: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.44	0.19	1.03	1.44	0.66	5.25	5.44	1.69	1.35	ns
4 mA	STD	0.97	4.44	0.19	1.03	1.44	0.66	4.37	4.44	1.99	2.11	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.5V DC core voltage for the 1.8V LVCMOS high slew commercial-case conditions.

TABLE 2-54: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.64	0.19	1.03	1.44	0.66	2.59	2.64	1.69	1.40	ns
4 mA	STD	0.97	2.08	0.19	1.03	1.44	0.66	2.12	1.95	1.99	2.19	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.4.2 Timing Characteristics: Applies to 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.8V LVCMOS low slew commercial-case conditions.

TABLE 2-55: 1.8V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	5.92	0.26	1.13	1.59	1.10	5.72	5.92	2.11	1.95	ns
4 mA	STD	1.55	4.91	0.26	1.13	1.59	1.10	4.82	4.91	2.42	2.73	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.8V LVCMOS high slew commercial-case conditions.

TABLE 2-56: 1.8V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.7 V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	3.05	0.26	1.13	1.59	1.10	3.01	3.05	2.10	2.00	ns
4 mA	STD	1.55	2.49	0.26	1.13	1.59	1.10	2.53	2.34	2.42	2.81	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.5 1.5V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5V applications. It uses a 1.5V input buffer and a push-pull output buffer.

TABLE 2-57: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

1.5V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	I_{IL} [1]	I_{IH} [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Note 1: I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

2: IIH is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

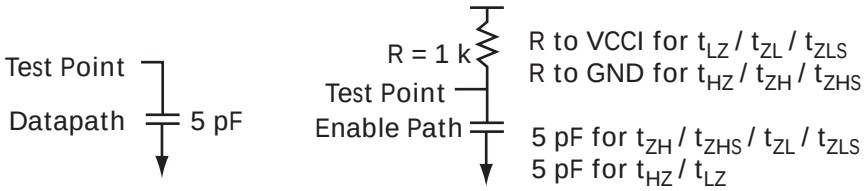
3: Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

4: Currents are measured at 85 °C junction temperature.

5: Software default selection highlighted in gray.

The following figure shows the C loading of 1.5V LVCMOS.

FIGURE 2-10: AC LOADING



The following table lists the 1.5V LVCMOS AC waveforms, measuring points, and capacitive loads.

TABLE 2-58: 1.5V LVCMOS AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

Note: *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

2.3.4.5.1 Timing Characteristics: Applies to 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the 1.5V LVCMOS low slew commercial-case conditions.

TABLE 2-59: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.5V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.4V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	5.39	0.19	1.19	1.62	0.66	5.48	5.39	2.02	2.06	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.5V DC core voltage for the 1.5V LVCMOS high slew commercial-case conditions.

TABLE 2-60: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.5V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V, WORST-CASE VCCI = 1.4V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	0.97	2.39	0.19	1.19	1.62	0.66	2.44	2.24	2.02	2.15	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.5.2 Timing Characteristics: Applies to 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.5V LVCMOS low slew commercial-case conditions.

TABLE 2-61: 1.5V LVCMOS LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.4V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	5.87	0.26	1.27	1.77	1.10	5.92	5.87	2.45	2.65	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.5V LVCMOS high slew commercial-case conditions.

TABLE 2-62: 1.5V LVCMOS HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.4V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	STD	1.55	2.78	0.26	1.27	1.77	1.10	2.82	2.62	2.44	2.74	ns

Note 1: Software default selection highlighted in gray.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.6 1.2V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2V complies with the LVCMOS standard JESD8-12A for general purpose 1.2V applications. It uses a 1.2V input buffer and a push-pull output buffer. The following table lists the minimum and maximum DC input and output levels for 1.2V LVCMOS.

TABLE 2-63: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

1.2V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
1 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1	10	13	10	10

Note 1: I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

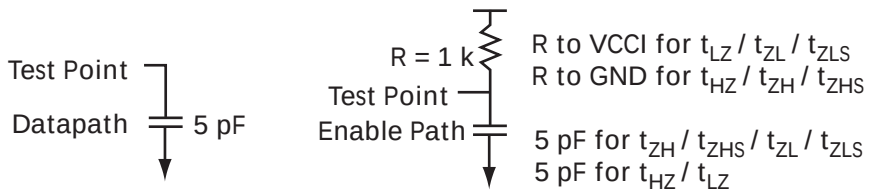
2: I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3: Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

4: Currents are measured at 85 °C junction temperature.

5: Software default selection highlighted in gray.

FIGURE 2-11: AC LOADING



The following table lists the 1.2V LVCMOS AC waveforms, measuring Points, and capacitive loads.

TABLE 2-64: 1.2V LVCMOS AC WAVEFORMS, MEASURING POINTS, AND CAPACITIVE LOADS

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-23 for a complete table of trip points.

2.3.4.6.1 Timing Characteristics: Applies to 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.2V LVCMOS low slew commercial-case conditions.

TABLE 2-65: 1.2V LVCMOS LOW SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.14V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	STD	1.55	8.30	0.26	1.56	2.27	1.10	7.97	7.54	2.56	2.55	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.2V LVCMOS low high commercial-case conditions.

TABLE 2-66: 1.2V LVCMOS HIGH SLEW COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.14V

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	STD	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.4.6.2 1.2V LVCMOS Wide Range

The following table lists the minimum and maximum DC input and output levels for the 1.2V LVCMOS wide range.

TABLE 2-67: MINIMUM AND MAXIMUM DC INPUT AND OUTPUT LEVELS

1.2V LVCMOS Wide Range	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
1 mA	–0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI – 0.1	100	100	10	13	10	10

Note 1: I_{IL} is the input leakage current per I/O pin over recommended operating conditions where –0.3 < VIN < VIL.

2: I_{IH} is the input leakage current per I/O pin over recommended operating conditions where VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3: Currents are measured at high temperature (100 °C junction temperature) and maximum voltage.

4: Currents are measured at 85 °C junction temperature.

5: Applicable to IGLOO nano V2 devices operating at VCCI ≥ VCC.

6: Software default selection highlighted in gray.

2.3.4.7 Timing Characteristics: Applies to 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.2V LVCMOS wide range low slew commercial-case conditions.

TABLE 2-68: 1.2V LVCMOS WIDE RANGE LOW SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.14V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	1 mA	STD	1.55	8.30	0.26	1.56	2.27	1.10	7.97	7.54	2.56	2.55	ns

Note 1: The minimum drive strength for any LVCMOS 1.2 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: For specific junction temperature and voltage supply levels, see <link>Table 2-6 2-20 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the 1.2V LVCMOS wide range high slew commercial-case conditions.

TABLE 2-69: 1.2V LVCMOS WIDE RANGE HIGH SLEW – APPLIES TO 1.2V DC CORE VOLTAGE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V, WORST-CASE VCCI = 1.14V

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	1 mA	STD	1.55	3.50	0.26	1.56	2.27	1.10	3.37	3.10	2.55	2.66	ns

Note 1: The minimum drive strength for any LVCMOS 1.2V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, see the IBIS models.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

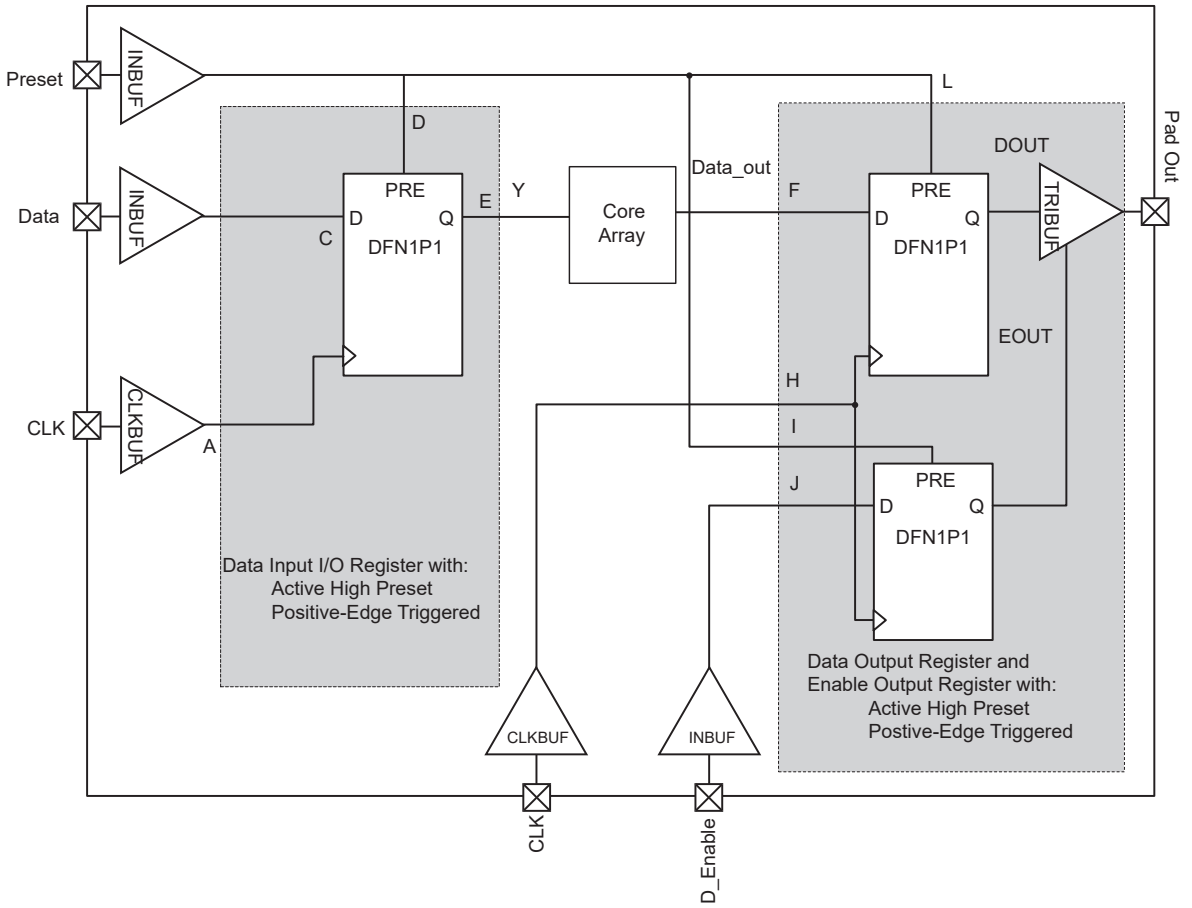
3: Software default selection highlighted in gray.

2.3.5 I/O REGISTER SPECIFICATIONS

2.3.5.1 Fully Registered I/O Buffers with Asynchronous Preset

The following figure shows the timing model for the fully registered I/O buffers with asynchronous preset.

FIGURE 2-12: TIMING MODEL OF REGISTERED I/O BUFFERS WITH ASYNCHRONOUS PRESET



The following table lists the parameter definition and measuring nodes fully registered I/O buffers with asynchronous preset.

TABLE 2-70: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)[1]
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A

TABLE 2-70: PARAMETER DEFINITION AND MEASURING NODES

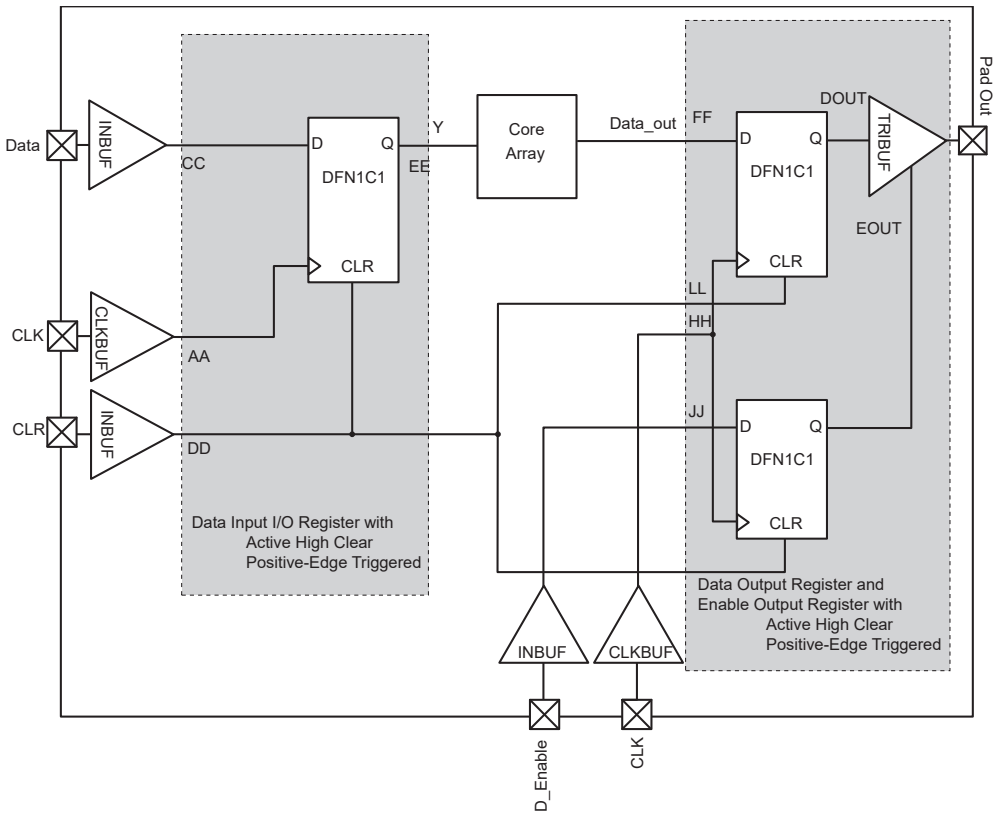
Parameter Name	Parameter Definition	Measuring Nodes (from, to)[1]
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

1. For more information, see Figure 2-12.

2.3.5.2 Fully Registered I/O Buffers with Asynchronous Clear

The following figure shows the timing model of the registered I/O buffer with asynchronous clear.

FIGURE 2-13: TIMING MODEL OF THE REGISTERED I/O BUFFERS WITH ASYNCHRONOUS CLEAR



The following table lists the parameter definition and measuring nodes.

TABLE 2-71: PARAMETER DEFINITION AND MEASURING NODES

Parameter Name	Parameter Definition	Measuring Nodes (from, to)[1]
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH

TABLE 2-71: PARAMETER DEFINITION AND MEASURING NODES

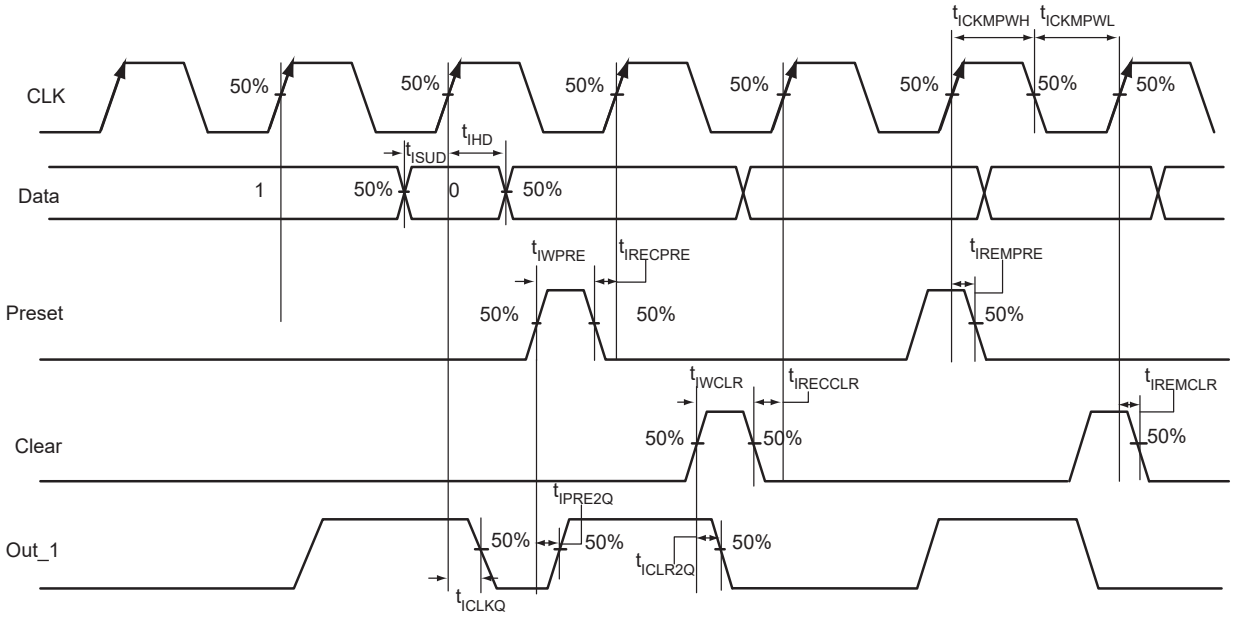
Parameter Name	Parameter Definition	Measuring Nodes (from, to)[1]
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

1. For more information, see Figure 2-13.

2.3.5.3 Input Register

The following figure shows the input register timing diagram.

FIGURE 2-14: INPUT REGISTER TIMING DIAGRAM



2.3.5.3.1 Timing Characteristics: 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the input data register propagation delays commercial-case conditions.

TABLE 2-72: INPUT DATA REGISTER PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns

TABLE 2-72: INPUT DATA REGISTER PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.5.3.2 Timing Characteristics: 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the input data register propagation delays commercial-case conditions

TABLE 2-73: INPUT DATA REGISTER PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

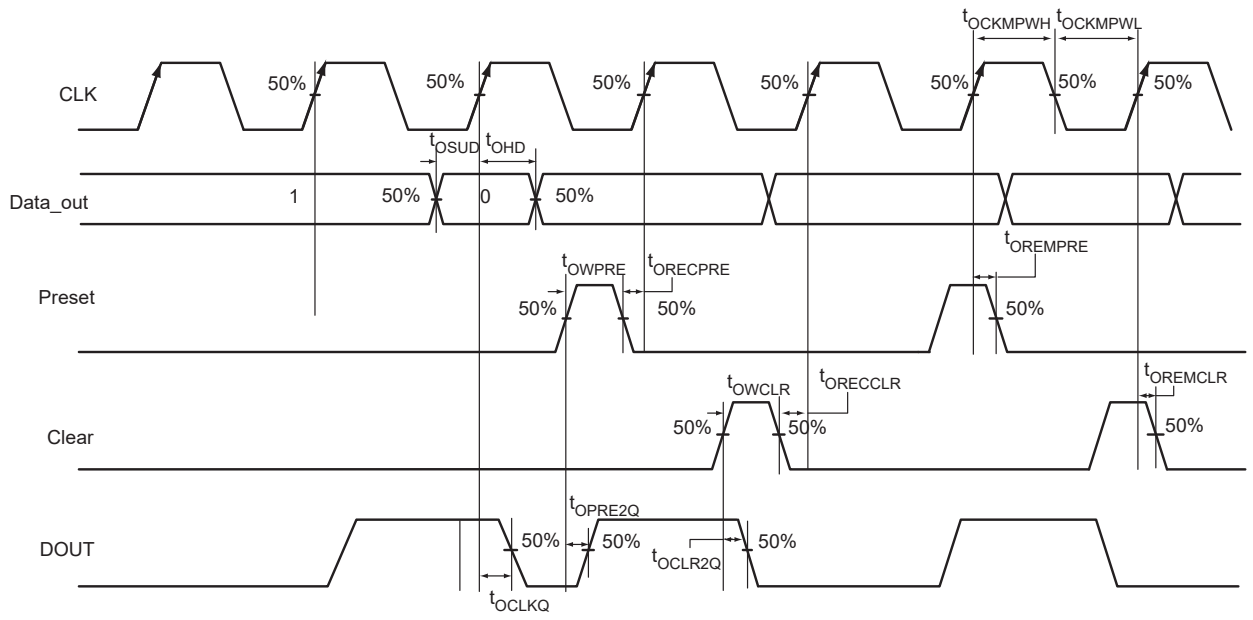
Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.68	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.97	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.3.5.4 Output Register

The following figure shows the output register timing diagram.

FIGURE 2-15: OUTPUT REGISTER TIMING DIAGRAM



2.3.5.4.1 Timing Characteristics: 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the output data register propagation delays commercial-case conditions

TABLE 2-74: OUTPUT DATA REGISTER PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.5.4.2 Timing Characteristics: 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the output data register propagation delays commercial-case conditions

TABLE 2-75: OUTPUT DATA REGISTER PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

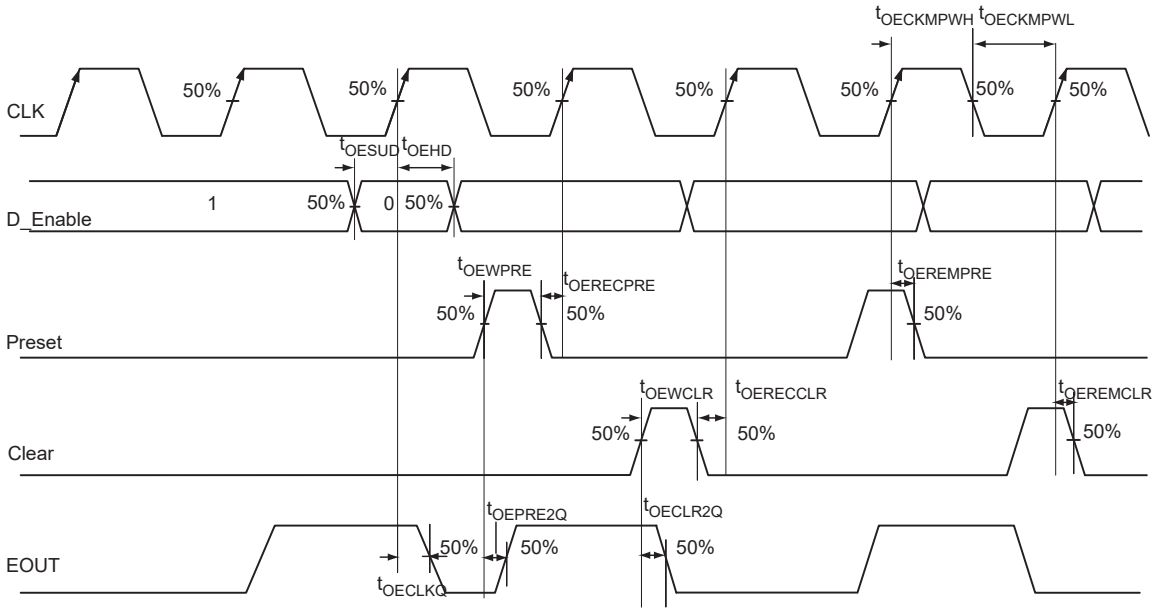
Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.3.5.5 Output Enable Register

The following figure shows the output enable register timing diagram.

FIGURE 2-16: OUTPUT ENABLE REGISTER TIMING DIAGRAM



2.3.5.5.1 *Timing Characteristics: 1.5V DC Core Voltage*

The following table lists the timing characteristics of 1.5V DC core voltage for the output enable register propagation delays commercial-case conditions.

TABLE 2-76: OUTPUT ENABLE REGISTER PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.75	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.5.5.2 *Timing Characteristics: 1.2V DC Core Voltage*

The following table lists the timing characteristics of 1.2V DC core voltage for the output enable register propagation delays commercial-case conditions.

TABLE 2-77: OUTPUT ENABLE REGISTER PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

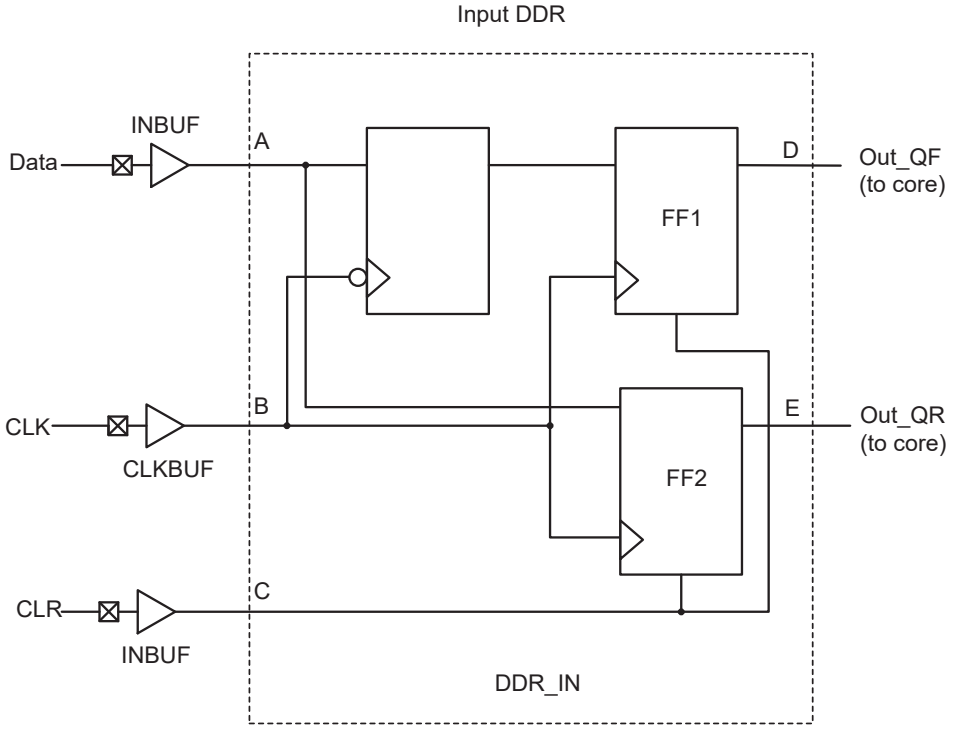
2.3.6 DDR MODULE SPECIFICATIONS

Note: DDR is not supported for AGLN010, AGLN015, and AGLN020 devices.

2.3.6.1 Input DDR Module

The following figure shows the input DDR model.

FIGURE 2-17: INPUT DDR TIMING MODEL



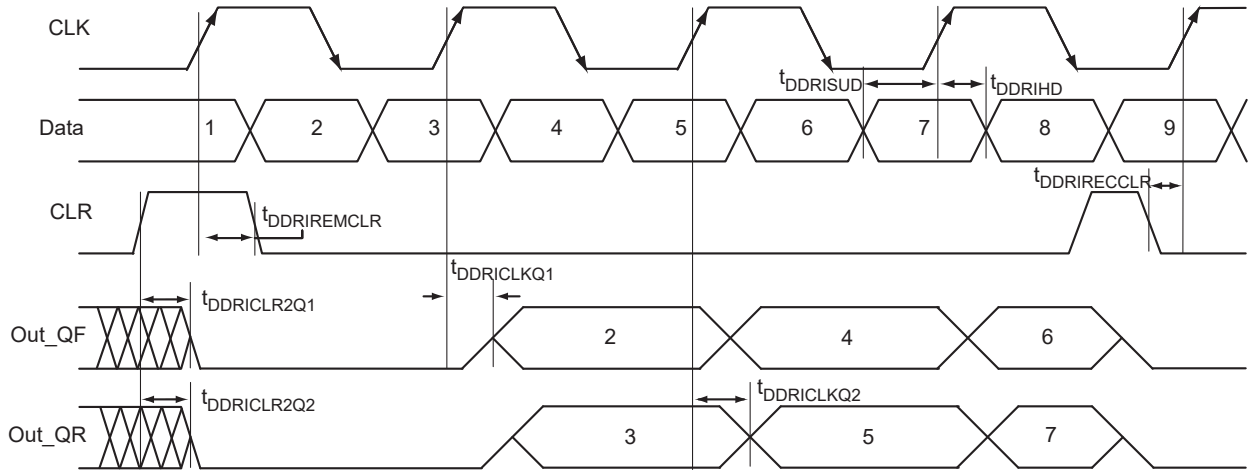
The following table lists the parameter definitions of the DDR module.

TABLE 2-78: PARAMETER DEFINITIONS

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

The following figure shows the input DDR timing diagram.

FIGURE 2-18: INPUT DDR TIMING DIAGRAM



2.3.6.1.1 Timing Characteristics: 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the input DDR propagation delays commercial-case conditions.

TABLE 2-79: INPUT DDR PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.25V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.3.6.1.2 Timing Characteristics: 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the input DDR propagation delays commercial-case conditions.

TABLE 2-80: INPUT DDR PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.94	ns

TABLE 2-80: INPUT DDR PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

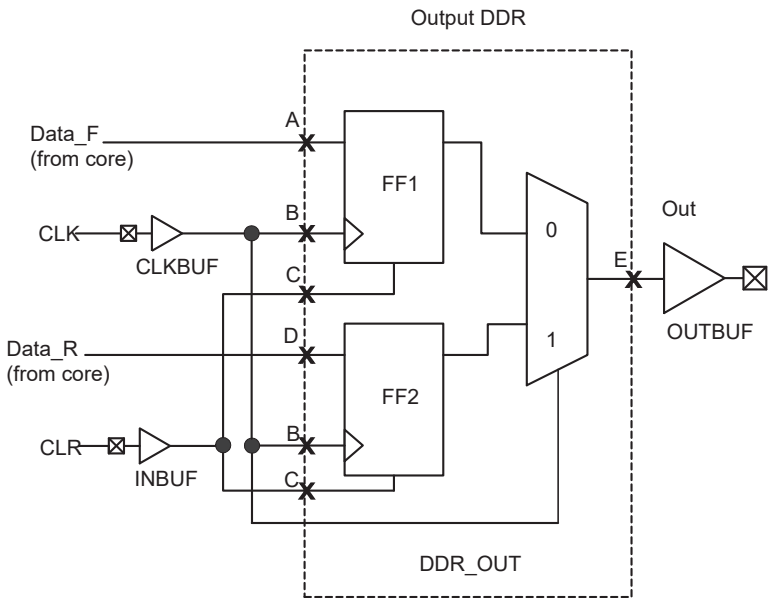
Parameter	Description	Std.	Units
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.84	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.3.6.2 Output DDR Module

The following figure shows the output DDR timing model.

FIGURE 2-19: OUTPUT DDR TIMING MODEL



The following table lists the parameter definitions for the output DDR timing model.

TABLE 2-81: PARAMETER DEFINITIONS

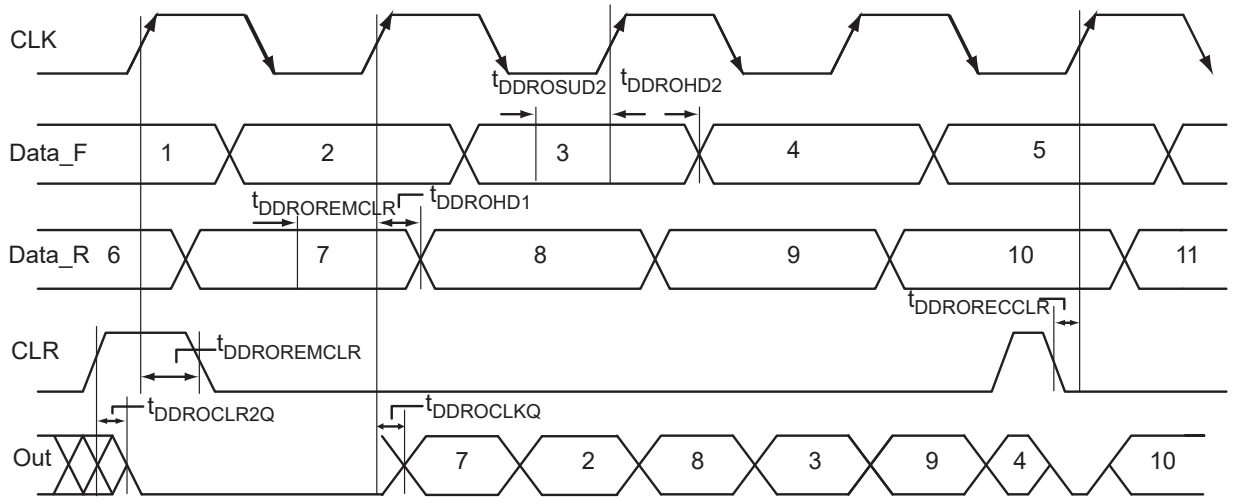
Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B

TABLE 2-81: PARAMETER DEFINITIONS

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

The following figure shows the output DDR timing diagram.

FIGURE 2-20: OUTPUT DDR TIMING DIAGRAM



2.3.6.2.1 Timing Characteristics: 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the output DDR propagation delays commercial-case conditions.

TABLE 2-82: OUTPUT DDR PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.3.6.2.2 Timing Characteristics:1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the output DDR propagation delays commercial-case conditions.

TABLE 2-83: OUTPUT DDR PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.4 VersaTile Characteristics

2.4.1 VERSATILE SPECIFICATIONS AS A COMBINATORIAL MODULE

The IGLOO nano library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, see the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for Software v10.1*.

FIGURE 2-21: SAMPLE OF COMBINATORIAL CELLS

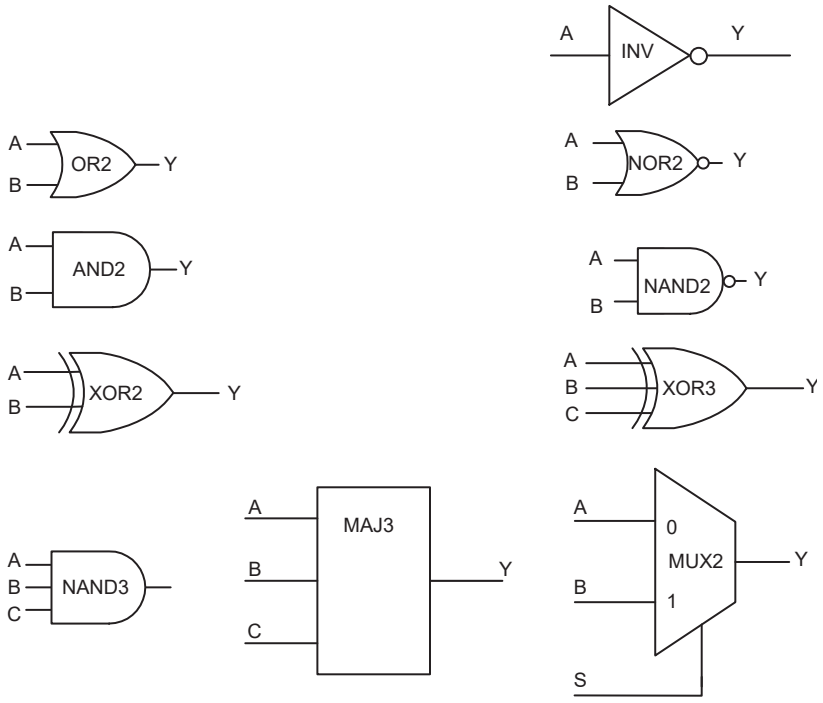
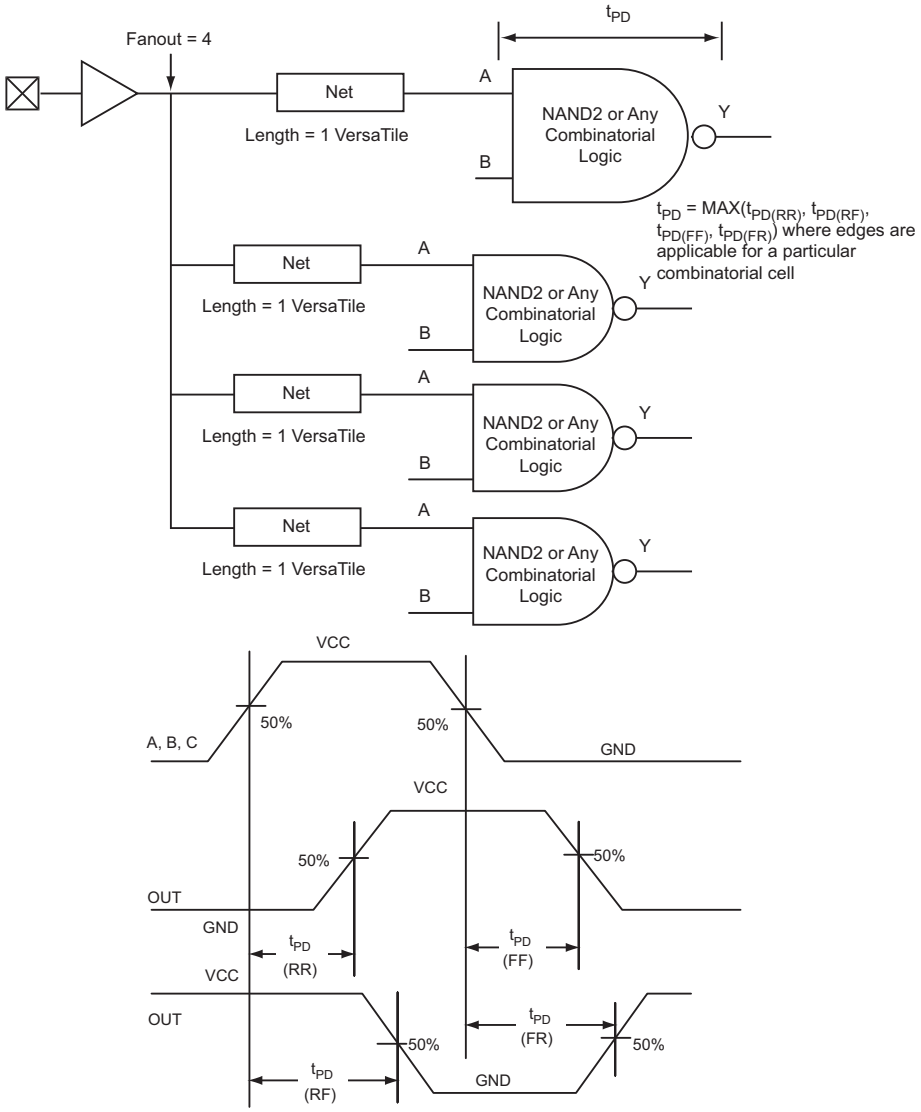


FIGURE 2-22: TIMING MODEL AND WAVEFORMS



2.4.1.1 Timing Characteristics: 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the combinatorial cell propagation delays commercial-case conditions.

TABLE 2-84: COMBINATORIAL CELL PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	0.76	ns
AND2	Y = A · B	t_{PD}	0.87	ns
NAND2	Y = !(A · B)	t_{PD}	0.91	ns
OR2	Y = A + B	t_{PD}	0.90	ns
NOR2	Y = !(A + B)	t_{PD}	0.94	ns
XOR2	Y = A ⊕ B	t_{PD}	1.39	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.44	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.60	ns
MUX2	Y = A !S + B S	t_{PD}	1.17	ns

TABLE 2-84: COMBINATORIAL CELL PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Combinatorial Cell	Equation	Parameter	Std.	Units
AND3	Y = A · B · C	t_{PD}	1.18	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.4.1.2 Timing Characteristics: 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the combinatorial cell propagation delays commercial-case conditions.

TABLE 2-85: COMBINATORIAL CELL PROPAGATION DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.33	ns
AND2	Y = A · B	t_{PD}	1.48	ns
NAND2	Y = !(A · B)	t_{PD}	1.58	ns
OR2	Y = A + B	t_{PD}	1.53	ns
NOR2	Y = !(A + B)	t_{PD}	1.63	ns
XOR2	Y = A ⊕ B	t_{PD}	2.34	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.59	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	2.74	ns
MUX2	Y = A !S + B S	t_{PD}	2.03	ns
AND3	Y = A · B · C	t_{PD}	2.11	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.4.2 VERSATILE SPECIFICATIONS AS A SEQUENTIAL MODULE

The IGLOO nano library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, see *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for Software v10.1*.

FIGURE 2-23: SAMPLE OF SEQUENTIAL CELLS

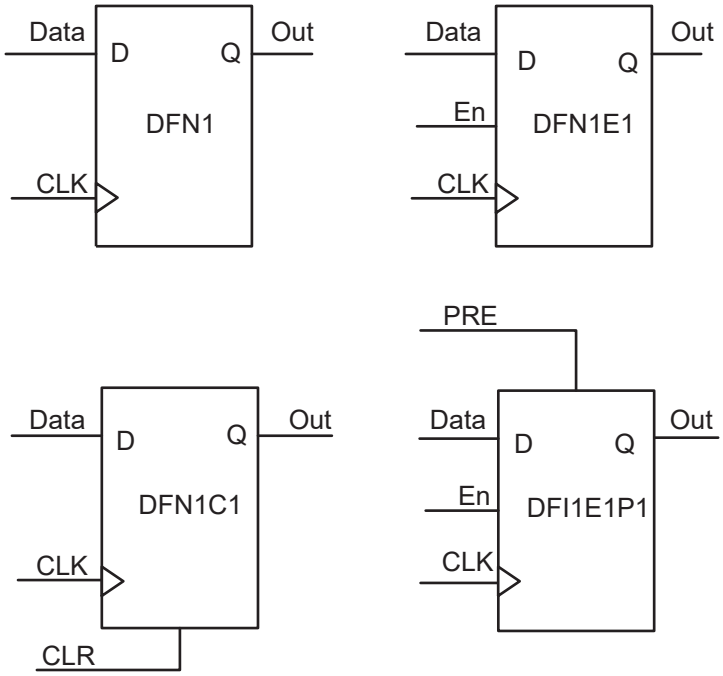
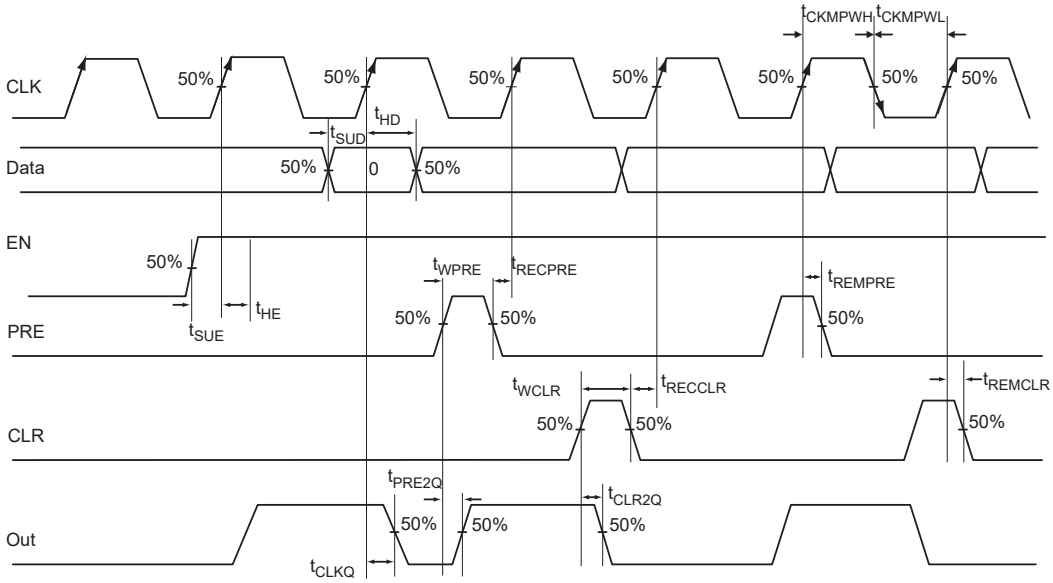


FIGURE 2-24: TIMING MODEL AND WAVEFORMS



2.4.2.1 Timing Characteristics: 1.5V DC Core Voltage

The following table lists the timing characteristics of 1.5V DC core voltage for the register delays commercial-case conditions.

TABLE 2-86: REGISTER DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns

TABLE 2-86: REGISTER DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.4.2.2 Timing Characteristics: 1.2V DC Core Voltage

The following table lists the timing characteristics of 1.2V DC core voltage for the register delays commercial-case conditions.

TABLE 2-87: REGISTER DELAYS COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.95	ns

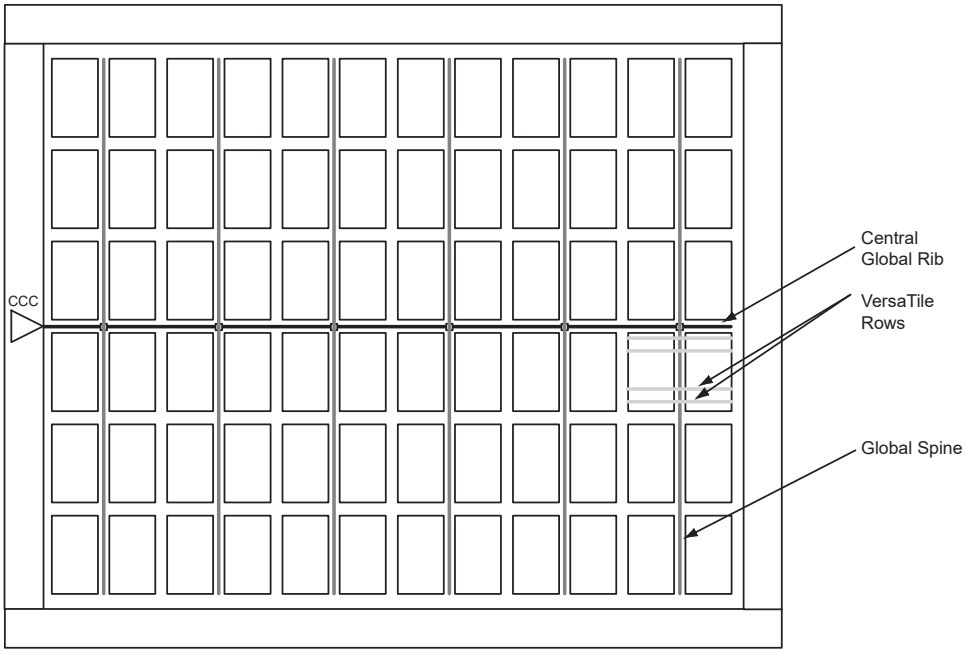
Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.5 Global Resource Characteristics

2.5.1 AGLN125 CLOCK TREE TOPOLOGY

Clock delays are device-specific. The following figure is an example of a global tree used for clock routing. The global tree presented in the following figure is driven by a CCC located on the west side of the AGLN125 device. It is used to drive all D-flip-flops in the device.

FIGURE 2-25: EXAMPLE OF GLOBAL TREE USE IN AN AGLN125 DEVICE FOR CLOCK ROUTING



2.5.2 GLOBAL TREE TIMING CHARACTERISTICS

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, see the section 2 "Clock Conditioning Circuits" . Table 2-88 to Table 2-96 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

2.5.2.1 Timing Characteristics: 1.5V DC Core Voltage

The following tables list the timing characteristics for the different devices for 1.5V DC core voltage.

TABLE 2-88: AGLN010 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.13	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.15	1.50	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.35	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element,

located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

TABLE 2-89: AGLN015 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.55	ns
t_{RCKH}	Input HIgh Delay for Global Clock	1.23	1.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.42	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

TABLE 2-90: AGLN020 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.42	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

TABLE 2-91: AGLN060 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.32	1.62	ns
t_{RCKH}	Input High Delay for Global Clock	1.34	1.71	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.38	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

TABLE 2-92: AGLN125 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.43	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

TABLE 2-93: AGLN250 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.43	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.5.2.2 Timing Characteristics: 1.2V DC Core Voltage

The following tables list the timing characteristics for the different devices for 1.2V DC core voltage.

TABLE 2-94: AGLN010 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.71	2.09	ns
t_{RCKH}	Input High Delay for Global Clock	1.78	2.31	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.53	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element,

located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

TABLE 2-95: AGLN015 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.81	2.26	ns
t_{RCKH}	Input High Delay for Global Clock	1.90	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.61	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

TABLE 2-96: AGLN020 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.81	2.26	ns
t_{RCKH}	Input High Delay for Global Clock	1.90	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.61	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, Table 2-7 for derating values.

TABLE 2-97: AGLN060 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.02	2.42	ns
t_{RCKH}	Input High Delay for Global Clock	2.09	2.65	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.56	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

TABLE 2-98: AGLN125 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.62	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

TABLE 2-99: AGLN250 GLOBAL RESOURCE COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.11	2.57	ns
t_{RCKH}	Input High Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40	—	ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65	—	ns
t_{RCKSW}	Maximum Skew for Global Clock	—	0.62	ns

Note 1: Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2: Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

2.6 Clock Conditioning Circuits

2.6.1 CCC ELECTRICAL SPECIFICATIONS

The following table lists the IGLOO nano CCC/PLL timing specification for IGLOO nano V2 or V5 devices at 1.5V DC core supply voltage.

TABLE 2-100: IGLOO NANO CCC/PLL SPECIFICATION FOR IGLOO NANO V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5	—	250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75	—	250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]	—	—	360[3]	—	ps
Number of Programmable Values in Each Programmable Delay Block		—	—	32	—
Serial Clock (SCLK) for Dynamic PLL [4,9]	—	—	—	100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)	—	—	—	1	ns

TABLE 2-100: IGLOO NANO CCC/PLL SPECIFICATION FOR IGLOO NANO V2 OR V5 DEVICES, 1.5V DC CORE SUPPLY VOLTAGE (CONTINUED)

Parameter		Min.	Typ.	Max.	Units
Acquisition Time	—	—	—	—	—
	LockControl = 0	—	—	300	µs
	LockControl = 1	—	—	6.0	ms
Tracking Jitter [5]	—	—	—	—	—
	LockControl = 0	—	—	2.5	ns
	LockControl = 1	—	—	1.5	ns
Output Duty Cycle	—	48.5	—	51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	—	1.25	—	15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2,]	—	0.025	—	15.65	ns
Delay Range in Block: Fixed Delay [1, 2]	—	—	3.5	—	ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6]	Max Peak-to-Peak Jitter Data [6,7,8]				
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16	—
0.75 MHz to 50 MHz	0.50	0.60	0.80	1.20	%
50 MHz to 250 MHz	2.50	4.00	6.00	12.00	%

Note 1: This delay is a function of voltage and temperature. See Table 2-6 and Table 2-7 for deratings.

2: T_J = 25 °C, V**CC** = 1.5V

3: When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4: Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, see Table 2-6 and Table 2-7 for derating values.

5: Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

6: VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.

7: Measurements done with LVTTL 3.3V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.425V, VCCI = 3.3V, VQ/PQ/TQ type of packages, 20 pF load.

8: SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the *IGLOO nano FPGA Fabric User's Guide*.

9: The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.

The following table lists the IGLOO nano CCC/PLL timing specification for IGLOO nano V2 at 1.2V DC core supply voltage.

TABLE 2-101: IGLOO NANO CCC/PLL SPECIFICATION FOR IGLOO NANO V2 DEVICES, 1.2V DC CORE SUPPLY VOLTAGE

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	—	1.5	—	160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75	—	160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		—	580[3]	—	ps
Number of Programmable Values in Each Programmable Delay Block		—	—	32	—
Serial Clock (SCLK) for Dynamic PLL [4,9]	—	—	—	60	—
Input Cycle-to-Cycle Jitter (peak magnitude)	—	—	—	0.25	ns

TABLE 2-101: IGLOO NANO CCC/PLL SPECIFICATION FOR IGLOO NANO V2 DEVICES, 1.2V DC CORE SUPPLY VOLTAGE

Parameter		Min.	Typ.	Max.	Units
Acquisition Time	—	—	—	—	—
	LockControl = 0	—	—	300	µs
	LockControl = 1	—	—	6.0	ms
Tracking Jitter [5]		—	—	—	—
	LockControl = 0	—	—	4	ns
	LockControl = 1	—	—	3	ns
Output Duty Cycle	—	48.5	—	51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	—	2.3	—	20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	—	0.025	—	20.86	ns
Delay Range in Block: Fixed Delay [1, 2]	—	—	5.7	—	ns
VCO Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6]	—	Max Peak-to-Peak Period Jitter [6,7,8]			
	SSO ≤ 2	SSO ≤ 4	SSO ≤ 8	SSO ≤ 16	—
0.75 MHz to 50MHz	0.50	1.20	2.00	3.00	%
50 MHz to 100 MHz	2.50	5.00	7.00	15.00	%

Note 1: This delay is a function of voltage and temperature. See <link>Table 2-6 2-20 and <link>Table 2-7 2-20 for deratings.

2: T_J = 25 °C, V_{CC} = 1.2V.

3: When the CCC/PLL core is generated by Microchip core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.

4: Maximum value obtained for a STD speed grade device in Worst-Case Commercial conditions. For specific junction temperature and voltage supply levels, see Table 2-6 and Table 2-7 for derating values.

5: Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

6: VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT, regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps, no matter what the settings are for the output divider.

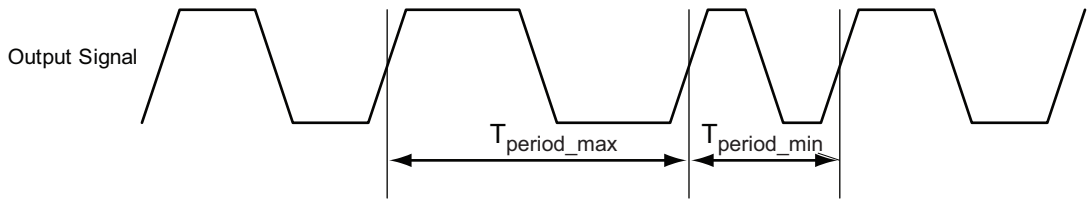
7: Measurements done with LVTTL 3.3 V 8 mA I/O drive strength and high slew rate. VCC/VCCPLL = 1.14 V, VCCI = 3.3 V, VQ/PQ/TQ type of packages, 20 pF load.

8: SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out times within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the *IGLOO nano FPGA Fabric User's Guide*.

9: The AGLN010, AGLN015, and AGLN020 devices do not support PLLs.

The following figure shows the timing diagram for the peak-to-peak jitter definition.

FIGURE 2-26: PEAK-TO-PEAK JITTER DEFINITION



Note: Peak-to-peak jitter measurements are defined by `Tpeak-to-peak = Tperiod_max - Tperiod_min`.

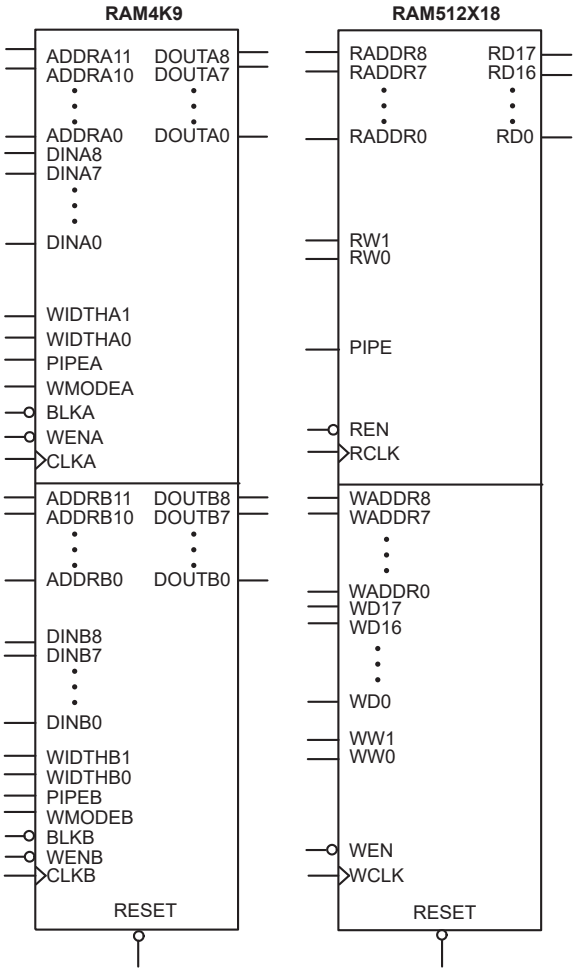
2.7 Embedded SRAM and FIFO Characteristics

The following sections describe the SRAM and FIFO characteristics.

2.8 SRAM

The following figure shows the SRAM model.

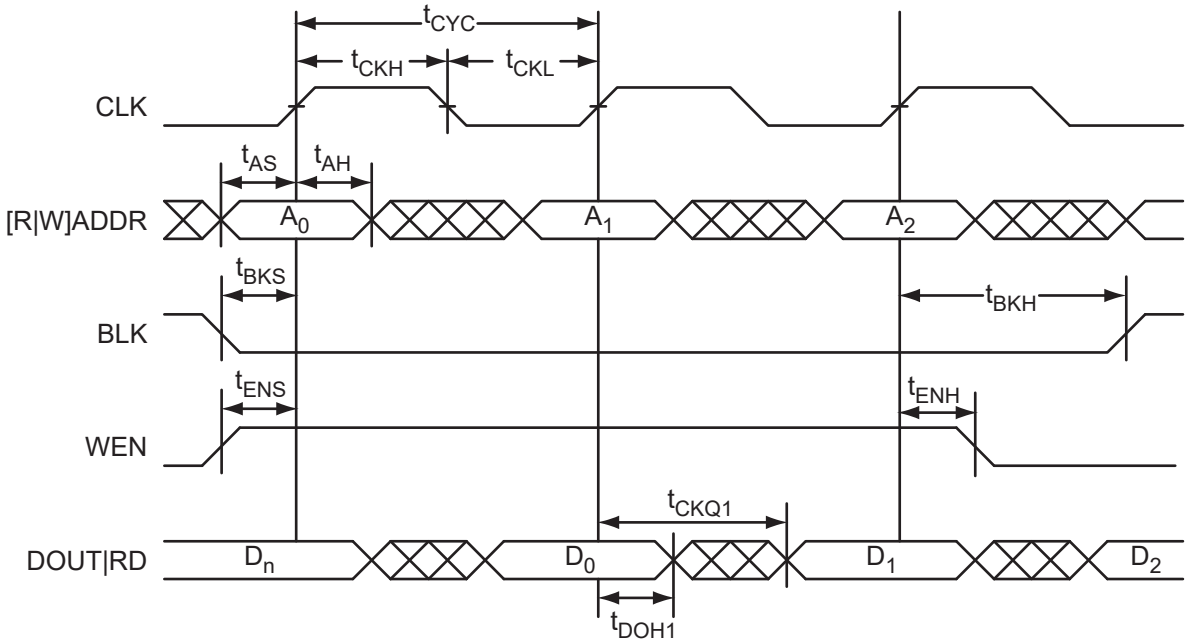
FIGURE 2-27: RAM MODELS



2.8.1 TIMING WAVEFORMS FOR EMBEDDED SRAM

The following figure shows the timing characteristics of RAM read for the pass-through output.

FIGURE 2-28: RAM READ FOR PASS-THROUGH OUTPUT (APPLICABLE TO BOTH RAM4K9 AND RAM512 X 18)



The following figure shows the timing characteristics of RAM read for pipelined output.

FIGURE 2-29: RAM READ FOR PIPELINED OUTPUT. APPLICABLE TO BOTH RAM4K9 AND RAM512 X 18

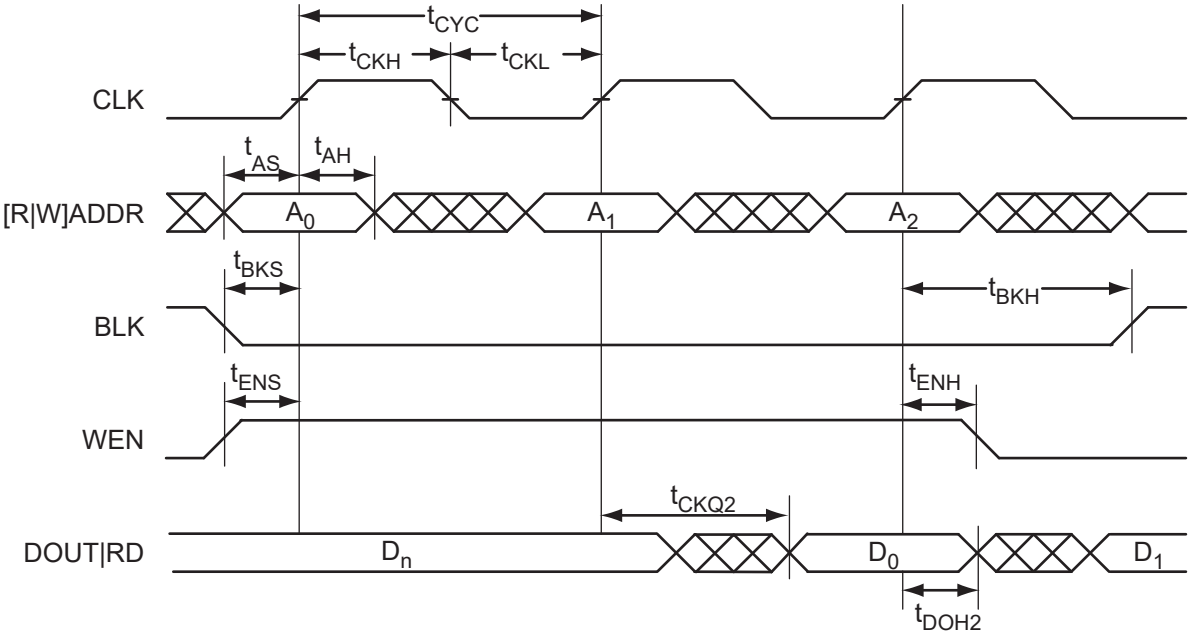


FIGURE 2-30: RAM WRITE, OUTPUT RETAINED (WMODE = 0). APPLICABLE TO BOTH RAM4K9 AND RAM512 X 18

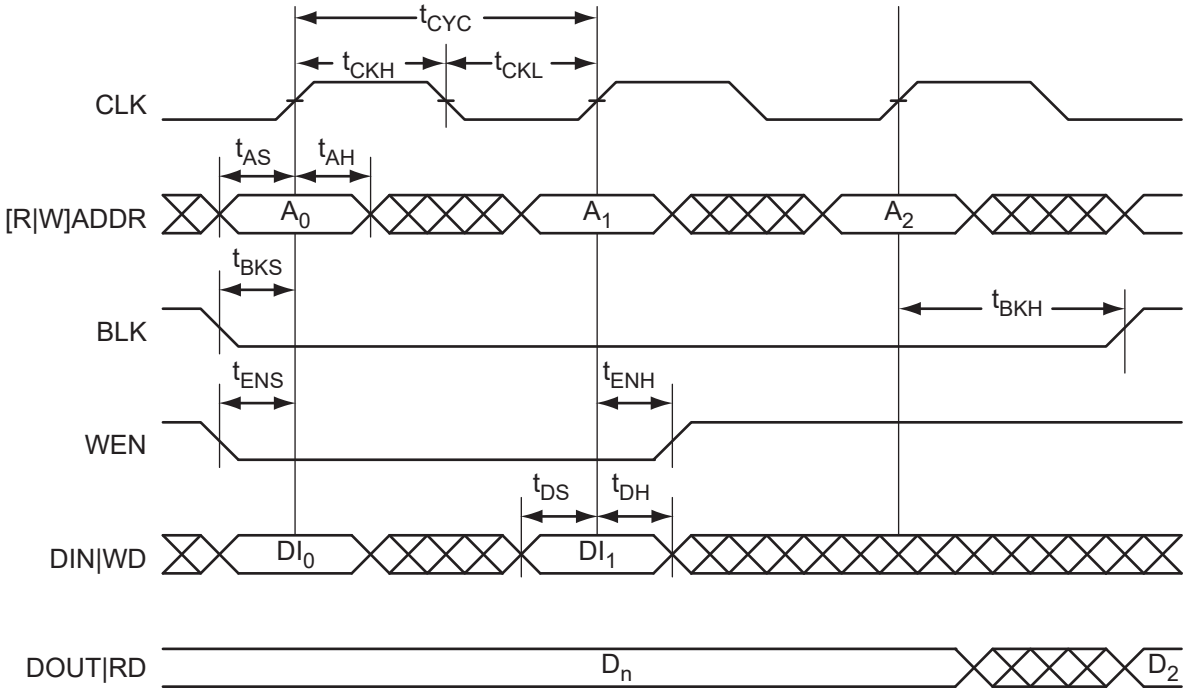


FIGURE 2-31: RAM WRITE, OUTPUT AS WRITE DATA (WMODE = 1). APPLICABLE TO RAM4K9 ONLY

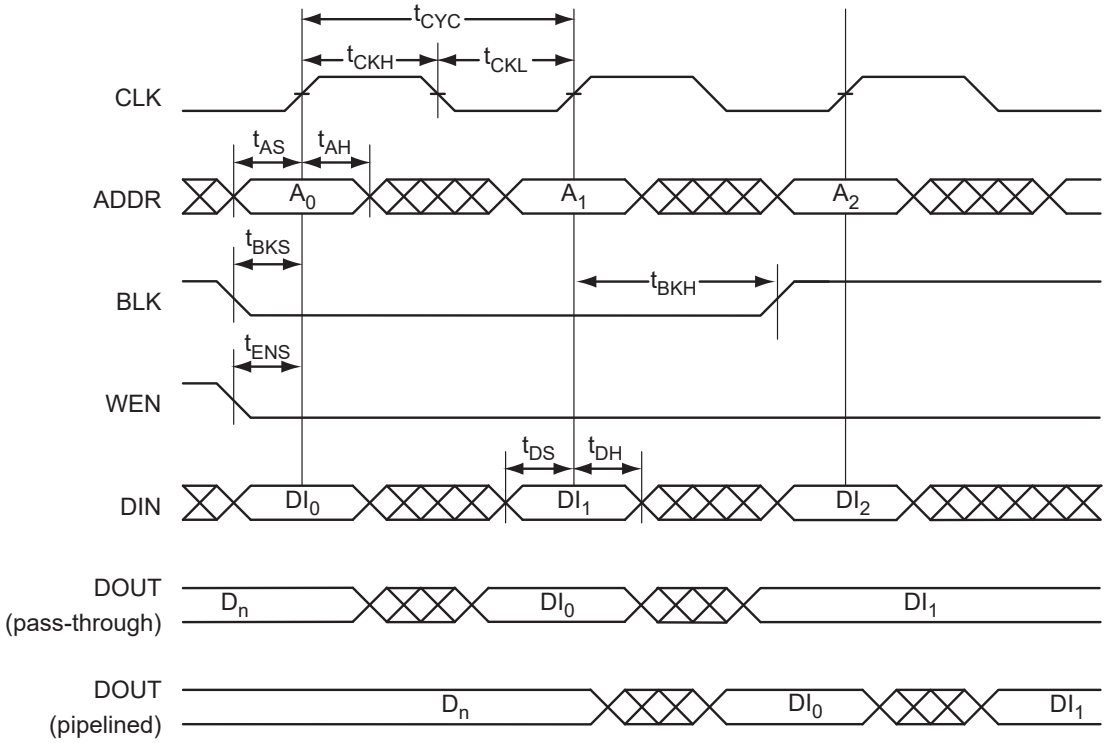
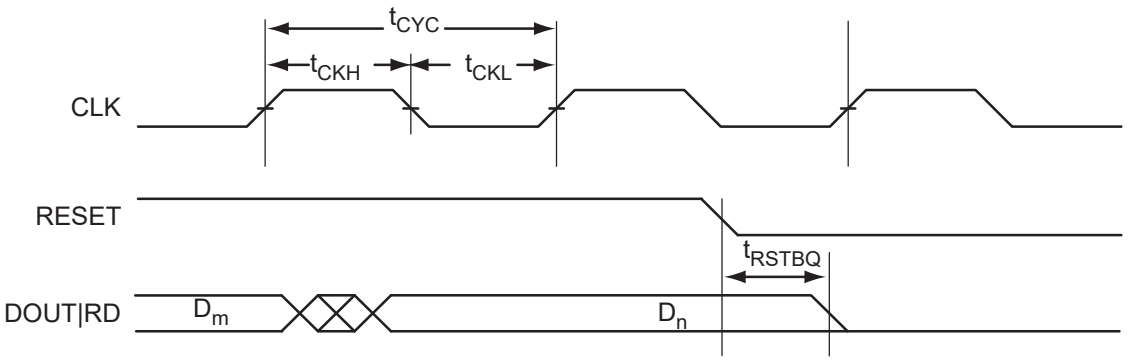


FIGURE 2-32: RAM RESET. APPLICABLE TO BOTH RAM4K9 AND RAM512 X 18



2.8.2 TIMING CHARACTERISTICS: 1.5V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.5V DC core voltage for the RAM4K9 commercial-case conditions.

TABLE 2-102: RAM4K9 COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.68	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{BKS}	BLK setup time	1.37	ns
t_{BKH}	BLK hold time	0.13	ns
t_{DS}	Input data (DIN) setup time	0.59	ns
t_{DH}	Input data (DIN) hold time	0.30	ns
t_{CKQ1}	Clock HIGH to new data valid on DOUT (output retained, WMODE = 0)	2.94	ns
	Clock HIGH to new data valid on DOUT (flow-through, WMODE = 1)	2.55	ns
t_{CKQ2}	Clock HIGH to new data valid on DOUT (pipelined)	1.51	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.23	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.41	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	1.72	ns
	RESET Low to data out Low on DOUT (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	ns
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note 1: For more information, see the application note *AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note*.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

The following table lists the timing characteristics of 1.5V DC core voltage for the RAM512 X 18 commercial-case conditions.

TABLE 2-103: RAM512 X 18 COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.69	ns
t_{AH}	Address hold time	0.13	ns
t_{ENS}	REN, WEN setup time	0.61	ns
t_{ENH}	REN, WEN hold time	0.07	ns
t_{DS}	Input data (WD) setup time	0.59	ns
t_{DH}	Input data (WD) hold time	0.30	ns
t_{CKQ1}	Clock HIGH to new data valid on RD (output retained)	3.51	ns
t_{CKQ2}	Clock HIGH to new data valid on RD (pipelined)	1.43	ns
t_{C2CRWH} [1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.35	ns
t_{C2CWRH} [1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	1.72	ns
	RESET Low to data out Low on RD (pipelined)	1.72	ns
$t_{REMRSTB}$	RESET removal	0.51	0.51
$t_{RECRSTB}$	RESET recovery	2.68	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note 1: For more information, see the *AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note*.

2: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.8.3 TIMING CHARACTERISTICS: 1.2V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.2V DC core voltage for the RAM4K9 commercial-case conditions.

TABLE 2-104: RAM4K9 COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.25	ns
t_{ENH}	REN, WEN hold time	0.25	ns
t_{BKS}	BLK setup time	2.54	ns
t_{BKH}	BLK hold time	0.25	ns
t_{DS}	Input data (DIN) setup time	1.10	ns
t_{DH}	Input data (DIN) hold time	0.55	ns
t_{CKQ1}	Clock HIGH to new data valid on DOUT (output retained, WMODE = 0)	5.51	ns
	Clock HIGH to new data valid on DOUT (flow-through, WMODE = 1)	4.77	ns
t_{CKQ2}	Clock HIGH to new data valid on DOUT (pipelined)	2.82	ns
t_{C2CWWL} [1]	Address collision clk-to-clk delay for reliable write after write on same address; applicable to closing edge	0.30	ns

TABLE 2-104: RAM4K9 COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.89	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.01	ns
t_{RSTBQ}	RESET LOW to data out LOW on DOUT (flow-through)	3.21	ns
	RESET LOW to data out LOW on DO (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Note 1: For more information, see the *AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note*.

2: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.

The following table lists the timing characteristics of 1.2V DC core voltage for the RAM512X18 commercial-case conditions.

TABLE 2-105: RAM512 X 18 COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.28	ns
t_{AH}	Address hold time	0.25	ns
t_{ENS}	REN, WEN setup time	1.13	ns
t_{ENH}	REN, WEN hold time	0.13	ns
t_{DS}	Input data (WD) setup time	1.10	ns
t_{DH}	Input data (WD) hold time	0.55	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	6.56	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	2.67	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address; applicable to opening edge	0.87	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address; applicable to opening edge	1.04	ns
t_{RSTBQ}	RESET LOW to data out LOW on RD (flow through)	3.21	ns
	RESET LOW to data out LOW on RD (pipelined)	3.21	ns
$t_{REMRSTB}$	RESET removal	0.93	ns
$t_{RECRSTB}$	RESET recovery	4.94	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

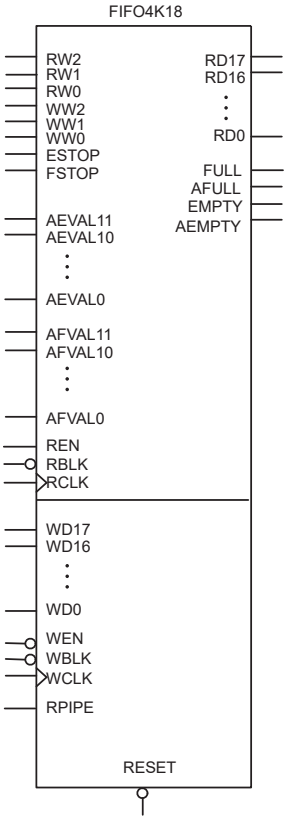
Note 1: For more information, see the application note *AC374: Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based FPGAs and SoC FPGAs App Note*.

2: For specific junction temperature and voltage supply levels, see <link>Table 2-7 2-20 for derating values.

2.9 FIFO

The following figure shows the FIFO model.

FIGURE 2-33: FIFO MODEL



2.9.1 TIMING WAVEFORMS FOR FIFO

The following figures shows the various FIFO timing waveforms.

FIGURE 2-34: FIFO READ

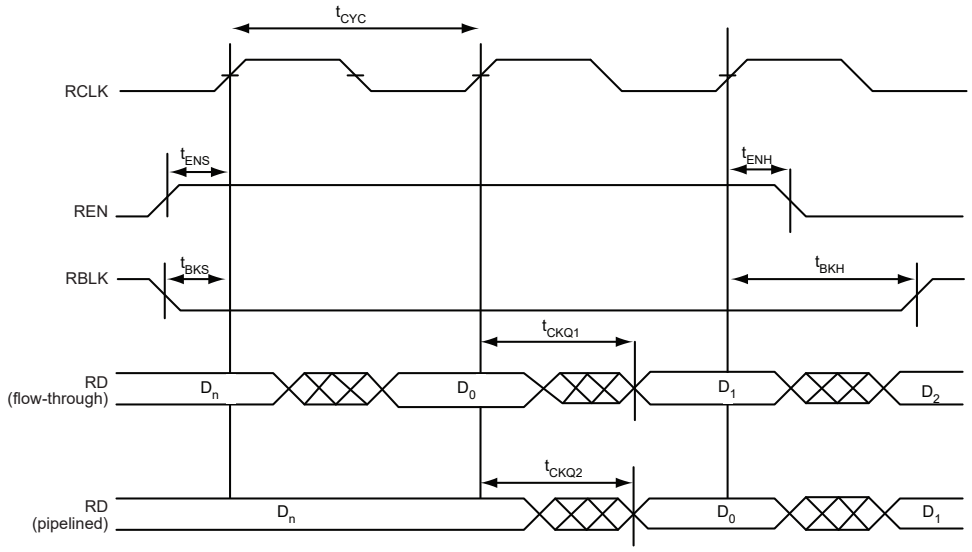


FIGURE 2-35: FIFO WRITE

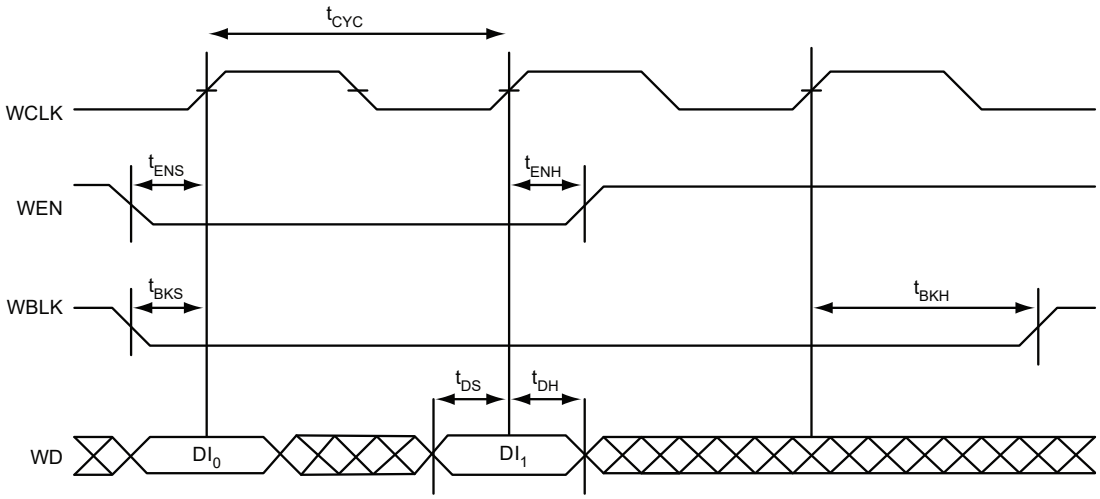


FIGURE 2-36: FIFO RESET

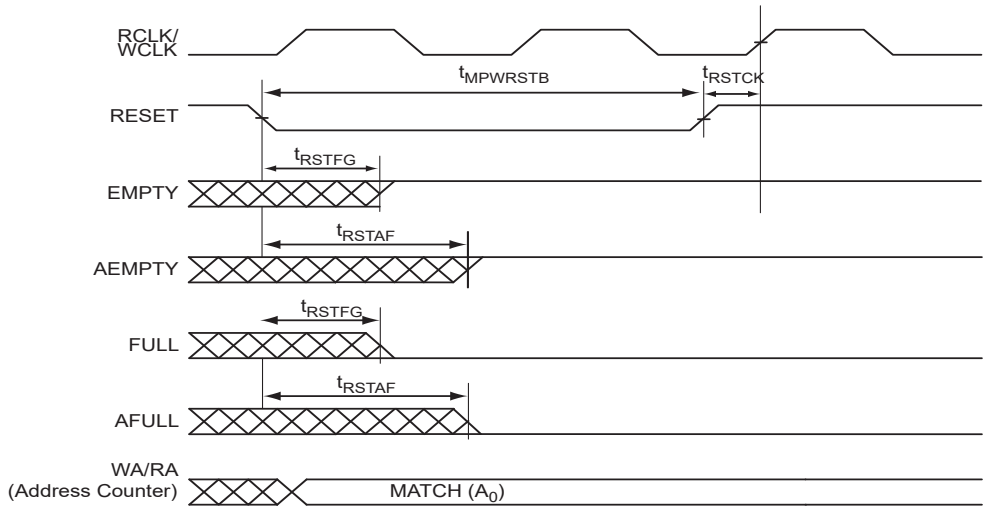


FIGURE 2-37: FIFO EMPTY FLAG AND AEMPTY FLAG ASSERTION

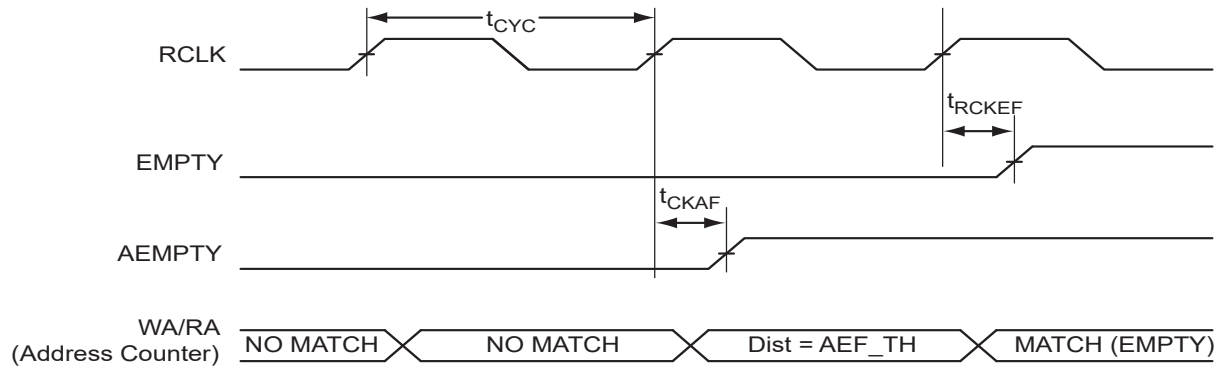


FIGURE 2-38: FIFO FULL FLAG AND AFULL FLAG ASSERTION

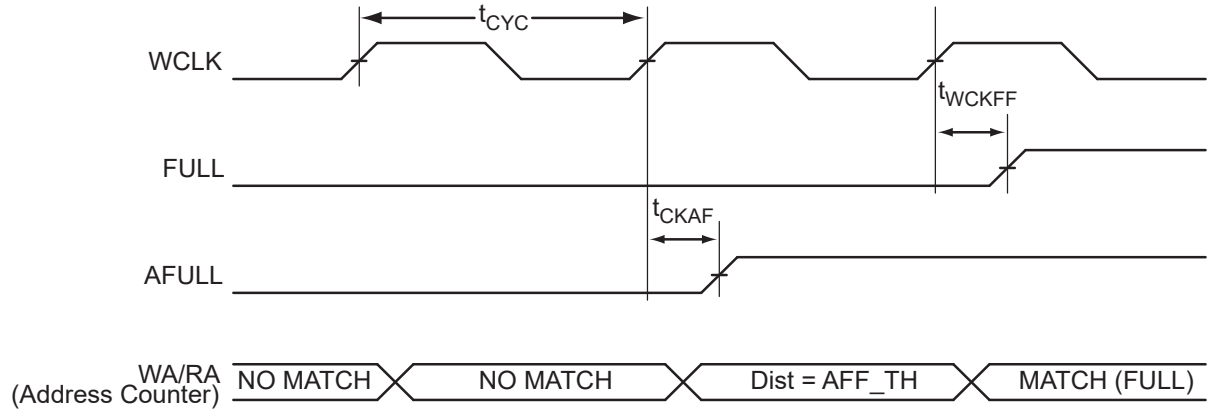


FIGURE 2-39: FIFO EMPTY FLAG AND AEMPTY FLAG DEASSERTION

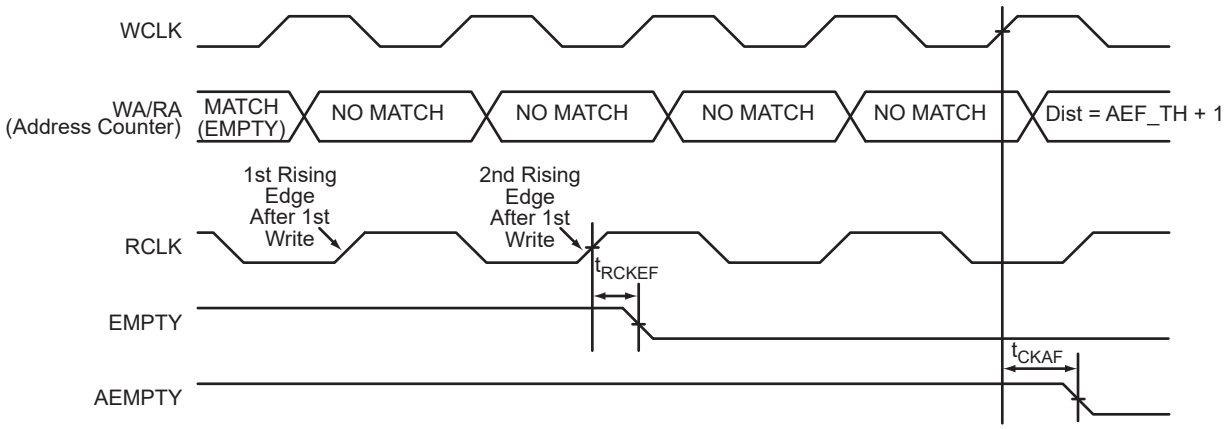
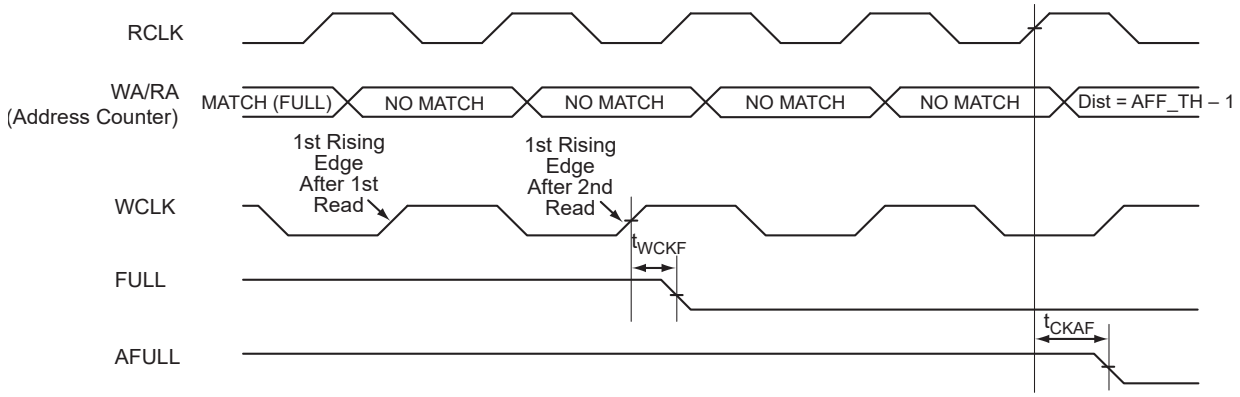


FIGURE 2-40: FIFO FULL FLAG AND AFULL FLAG DEASSERTION



2.9.2 TIMING CHARACTERISTICS: 1.5V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.5V DC core voltage for the FIFO worst commercial-case conditions.

TABLE 2-106: FIFO WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	ns

TABLE 2-106: FIFO WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.	Units
t_{ENH}	REN, WEN Hold Time	0.13	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.63	ns
t_{DH}	Input Data (WD) Hold Time	0.20	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.77	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.50	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	2.94	ns
t_{WCKFF}	WCLK High to Full Flag Valid	2.79	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	10.71	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	2.90	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	10.60	ns
t_{RSTBQ}	RESET Low to Data Out LOW on RD (flow-through)	1.68	ns
	RESET Low to Data Out LOW on RD (pipelined)	1.68	ns
$t_{REMRSTB}$	RESET Removal	0.51	ns
$t_{RECRSTB}$	RESET Recovery	2.68	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.9.3 TIMING CHARACTERISTICS: 1.2V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.2V DC core voltage for the FIFO worst commercial-case conditions.

TABLE 2-107: FIFO WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.44	ns
t_{ENH}	REN, WEN Hold Time	0.26	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.30	ns
t_{DH}	Input Data (DI) Hold Time	0.41	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	5.67	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.02	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	6.02	ns
t_{WCKFF}	WCLK High to Full Flag Valid	5.71	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	22.17	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	5.93	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	21.94	ns
t_{RSTBQ}	RESET LOW to Data Out Low on RD (flow-through)	3.41	ns
	RESET LOW to Data Out Low on RD (pipelined)	4.09	3.41
$t_{REMRSTB}$	RESET Removal	1.02	ns
$t_{RECRSTB}$	RESET Recovery	5.48	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	1.18	ns

TABLE 2-107: FIFO WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

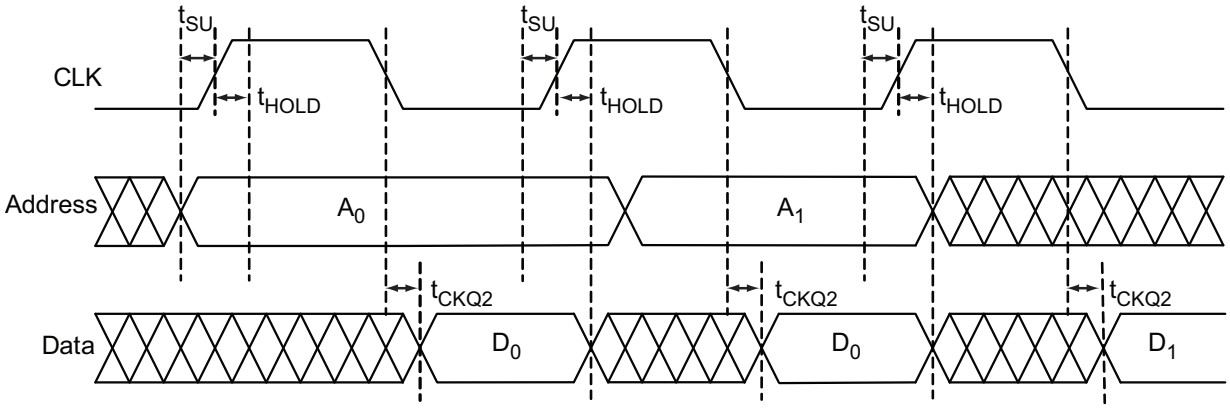
Parameter	Description	Std.	Units
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, see Table 2-7 for derating values.\

2.10 Embedded FlashROM Characteristics

The following figure shows the timing diagram of the embedded FlashROM.

FIGURE 2-41: TIMING DIAGRAM



2.10.1 TIMING CHARACTERISTICS—1.5V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.5V DC core voltage for the embedded FlashROM access time worst commercial-case conditions.

TABLE 2-108: EMBEDDED FLASHROM ACCESS TIME WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.425V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	20.90	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

2.10.2 TIMING CHARACTERISTICS—1.2V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.2V DC core voltage for the embedded FlashROM access time worst commercial-case conditions.

TABLE 2-109: EMBEDDED FLASHROM ACCESS TIME WORST COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, VCC = 1.14V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	35.74	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

2.11 JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; see the I/O timing characteristics in the section 2 "User I/O Characteristics" for more details.

2.11.1 TIMING CHARACTERISTICS—1.5V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.5V DC core voltage for the JTAG 1532 commercial-case conditions.

TABLE 2-110: JTAG 1532 COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.425V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

2.11.2 TIMING CHARACTERISTICS—1.2V DC CORE VOLTAGE

The following table lists the timing characteristics of 1.2V DC core voltage for the JTAG 1532 commercial-case conditions.

TABLE 2-111: JTAG 1532 COMMERCIAL-CASE CONDITIONS: T_J = 70 °C, WORST-CASE VCC = 1.14V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, see Table 2-6 for derating values.

3.0 PIN DESCRIPTIONS

3.1 Supply Pins

3.1.1 GND—GROUND

Ground supply voltage to the core, I/O outputs, and I/O logic.

3.1.2 GNDQ—GROUND (QUIET)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

3.1.3 VCC—CORE SUPPLY VOLTAGE

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO nano V5 devices, and 1.2V or 1.5V for IGLOO nano V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

3.1.4 VCCIBX—I /O SUPPLY VOLTAGE

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power Flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

3.1.5 VMVX—I/O SUPPLY VOLTAGE (QUIET)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

3.1.6 VCCPLA/B/C/D/E/F—PLL SUPPLY VOLTAGE

Supply voltage to analog PLL, nominally 1.5V or 1.2 V.

When the PLLs are not used, the Microchip Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microchip recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter in the *IGLOO nano FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on IGLOO nano devices.

3.1.7 VCOMPLA/B/C/D/E/F—PLL GROUND

Ground to analog PLL power supplies. When the PLLs are not used, the Microchip Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO nano devices.

3.1.8 VJTAG—JTAG SUPPLY VOLTAGE

Low power Flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.1.9 VPUMP—PROGRAMMING SUPPLY VOLTAGE

IGLOO nano devices support single-voltage ISP of the configuration Flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microchip recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

3.2 User Pins

3.2.1 I/O—USER INPUT/OUTPUT

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

3.2.2 GL—GLOBALS

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter in the *IGLOO nano FPGA Fabric User's Guide.* All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in nano Devices" chapter of the *IGLOO nano FPGA Fabric User's Guide* for an explanation of the naming of global pins.

3.2.3 FF—FLASH*FREEZE MODE ACTIVATION PIN

Flash*Freeze is available on IGLOO nano devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO nano devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO nano devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO nano FPGA Fabric User's Guide* for more information on I/O states during Flash*Freeze mode.

TABLE 3-1: FLASH*FREEZE PIN LOCATIONS FOR IGLOO NANO DEVICES

Package	Flash*Freeze Pin
CS81/UC81[1]	H2
QN48	14
QN68	18
VQ100	27
UC36	E2

Note 1: Package UC81 has been discontinued.

3.3 JTAG Pins

Low power Flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5V to 3.3V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

3.3.1 TCK—TEST CLOCK

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microchip recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

TABLE 3-2: RECOMMENDED TIE-OFF VALUES FOR THE TCK AND TRST PINS

VJTAG	Tie-Off Resistance [1,2]
VJTAG at 3.3V	200Ω to 1 kΩ
VJTAG at 2.5V	200Ω to 1 kΩ
VJTAG at 1.8V	500Ω to 1 kΩ
VJTAG at 1.5V	500Ω to 1 kΩ

Note 1: The TCK pin can be pulled-up or pulled-down.

2: The TRST pin is pulled-down.

3: Equivalent parallel resistance if more than one device is on the JTAG chain

TABLE 3-3: TRST AND TCK PULL-DOWN RECOMMENDATIONS

VJTAG	Tie-Off Resistance[1]
VJTAG at 3.3V	200 Ω to 1 kΩ
VJTAG at 2.5V	200 Ω to 1 kΩ
VJTAG at 1.8V	500 Ω to 1 kΩ
VJTAG at 1.5V	500 Ω to 1 kΩ

1. Equivalent parallel resistance if more than one device is on the JTAG chain

3.3.2 TDITEST—DATA INPUT

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

3.3.3 TDO—TEST DATA OUTPUT

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

3.3.4 TMS—TEST MODE SELECT

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

3.3.5 TRS—TBOUNDARY SCAN RESET PIN

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected through a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microchip recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

3.4 Special Function Pins

3.4.1 NC—NO CONNECT

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

3.4.2 DC—DO NOT CONNECT

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

3.5 Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

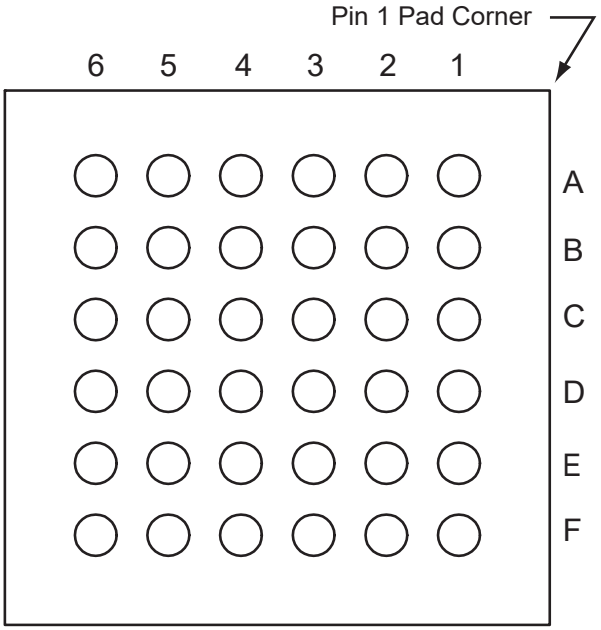
Microchip consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Microchip IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Microchip offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

4.0 PACKAGE PIN ASSIGNMENTS

4.1 UC36

This is the bottom view of the UC36 package.

FIGURE 4-1: UC36



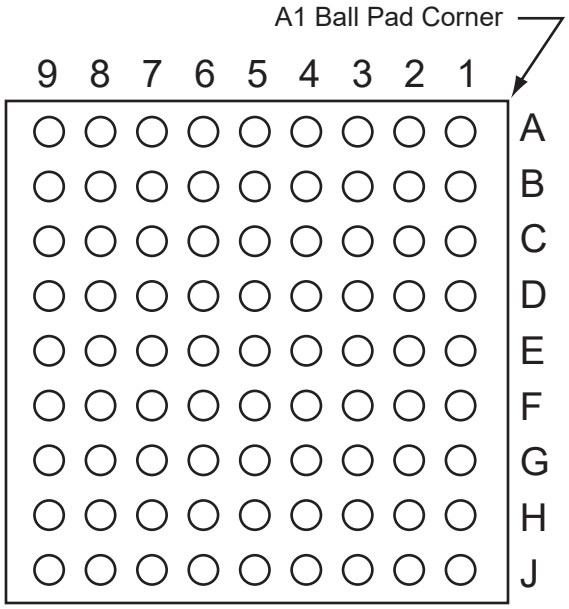
Note: For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/support/package-drawings/fpga-packaging.

UC36	
Pin Number	**AGLN010 Function**
A1	IO21RSB1
A2	IO18RSB1
A3	IO13RSB1
A4	GDC0/IO00RSB0
A5	IO06RSB0
A6	GDA0/IO04RSB0
B1	GEC0/IO37RSB1
B2	IO20RSB1
B3	IO15RSB1
B4	IO09RSB0
B5	IO08RSB0
B6	IO07RSB0
C1	IO22RSB1
C2	GEA0/IO34RSB1
C3	GND
C4	GND
C5	VCCIB0
C6	IO02RSB0
D1	IO33RSB1
D2	VCCIB1
D3	VCC
D4	VCC
D5	IO10RSB0
D6	IO11RSB0
E1	IO32RSB1
E2	FF/IO31RSB1
E3	TCK
E4	VPUMP
E5	TRST
E6	VJTAG
F1	IO29RSB1
F2	IO25RSB1
F3	IO23RSB1
F4	TDI
F5	TMS
F6	TDO

4.2 UC81

This is the bottom view of the UC81 package.

FIGURE 4-2: UC81



Note: For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/support/package-drawings/fpga-packaging.

UC81	
Pin Number	AGLN020 Function
A1	IO64RSB2
A2	IO54RSB2
A3	IO57RSB2
A4	IO36RSB1
A5	IO32RSB1
A6	IO24RSB1
A7	IO20RSB1
A8	IO04RSB0
A9	IO08RSB0
B1	IO59RSB2
B2	IO55RSB2
B3	IO62RSB2
B4	IO34RSB1
B5	IO28RSB1
B6	IO22RSB1
B7	IO18RSB1
B8	IO00RSB0
B9	IO03RSB0
C1	IO51RSB2
C2	IO50RSB2
C3	NC
C4	NC
C5	NC
C6	NC
C7	NC
C8	IO10RSB0
C9	IO07RSB0
D1	IO49RSB2
D2	IO44RSB2
D3	NC
D4	VCC
D5	VCCIB2
D6	GND
D7	NC
D8	IO13RSB0
D9	IO12RSB0
E1	GEC0/IO48RSB2
E2	GEA0/IO47RSB2
E3	NC
E4	VCCIB1
E5	VCC
E6	VCCIB0

UC81	
Pin Number	AGLN020 Function
E7	NC
E8	GDA0/IO15RSB0
E9	GDC0/IO14RSB0
F1	IO46RSB2
F2	IO45RSB2
F3	NC
F4	GND
F5	VCCIB1
F6	NC
F7	NC
F8	IO16RSB0
F9	IO17RSB0
G1	IO43RSB2
G2	IO42RSB2
G3	IO41RSB2
G4	IO31RSB1
G5	NC
G6	IO21RSB1
G7	NC
G8	VJTAG
G9	TRST
H1	IO40RSB2
H2	FF/IO39RSB1
H3	IO35RSB1
H4	IO29RSB1
H5	IO26RSB1
H6	IO25RSB1
H7	IO19RSB1
H8	TDI
H9	TDO
J1	IO38RSB1
J2	IO37RSB1
J3	IO33RSB1
J4	IO30RSB1
J5	IO27RSB1
J6	IO23RSB1
J7	TCK
J8	TMS
J9	VPUMP

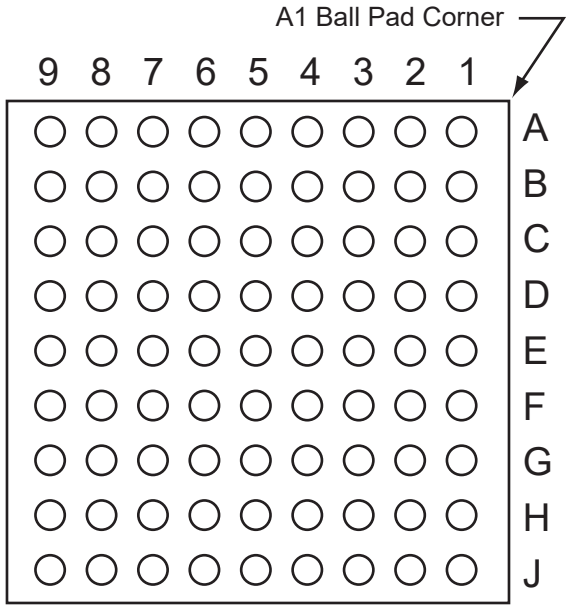
UC81	
Pin Number	AGLN030Z Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC

UC81	
Pin Number	**AGLN030Z Function**
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

4.3 CS81

This is the bottom view of the CS81 package.

FIGURE 4-3: CS81



Note: For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/support/package-drawings/fpga-packaging.

CS81	
Pin Number	AGLN020 Function
A1	IO64RSB2
A2	IO54RSB2
A3	IO57RSB2
A4	IO36RSB1
A5	IO32RSB1
A6	IO24RSB1
A7	IO20RSB1
A8	IO04RSB0
A9	IO08RSB0
B1	IO59RSB2
B2	IO55RSB2
B3	IO62RSB2
B4	IO34RSB1
B5	IO28RSB1
B6	IO22RSB1
B7	IO18RSB1
B8	IO00RSB0
B9	IO03RSB0
C1	IO51RSB2
C2	IO50RSB2
C3	NC
C4	NC
C5	NC
C6	NC
C7	NC
C8	IO10RSB0
C9	IO07RSB0
D1	IO49RSB2
D2	IO44RSB2
D3	NC
D4	VCC
D5	VCCIB2
D6	GND
D7	NC
D8	IO13RSB0
D9	IO12RSB0
E1	GEC0/IO48RSB2
E2	GEA0/IO47RSB2
E3	NC
E4	VCCIB1
E5	VCC

CS81	
Pin Number	AGLN020 Function
E6	VCCIB0
E7	NC
E8	GDA0/IO15RSB0
E9	GDC0/IO14RSB0
F1	IO46RSB2
F2	IO45RSB2
F3	NC
F4	GND
F5	VCCIB1
F6	NC
F7	NC
F8	IO16RSB0
F9	IO17RSB0
G1	IO43RSB2
G2	IO42RSB2
G3	IO41RSB2
G4	IO31RSB1
G5	NC
G6	IO21RSB1
G7	NC
G8	VJTAG
G9	TRST
H1	IO40RSB2
H2	FF/IO39RSB1
H3	IO35RSB1
H4	IO29RSB1
H5	IO26RSB1
H6	IO25RSB1
H7	IO19RSB1
H8	TDI
H9	TDO
J1	IO38RSB1
J2	IO37RSB1
J3	IO33RSB1
J4	IO30RSB1
J5	IO27RSB1
J6	IO23RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	AGLN030Z Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1

CS81	
Pin Number	**AGLN030Z Function**
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	**AGLN060 Function**
A1	GAA0/IO02RSB0
A2	GAA1/IO03RSB0
A3	GAC0/IO06RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO18RSB0
A7	GBB0/IO21RSB0
A8	GBA1/IO24RSB0
A9	GBA2/IO25RSB0
B1	GAA2/IO95RSB1
B2	GAB0/IO04RSB0
B3	GAC1/IO07RSB0
B4	IO08RSB0
B5	IO15RSB0
B6	GBC0/IO19RSB0
B7	GBB1/IO22RSB0
B8	IO26RSB0
B9	GBB2/IO27RSB0
C1	GAB2/IO93RSB1
C2	IO94RSB1
C3	GND
C4	IO10RSB0
C5	IO17RSB0
C6	GND
C7	GBA0/IO23RSB0
C8	GBC2/IO29RSB0
C9	IO31RSB0
D1	GAC2/IO91RSB1
D2	IO92RSB1
D3	GFA2/IO80RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO43RSB0
D8	GCC1/IO35RSB0
D9	GCC0/IO36RSB0
E1	GFB0/IO83RSB1
E2	GFB1/IO84RSB1
E3	GFA1/IO81RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0

CS81	
Pin Number	**AGLN060 Function**
E7	GCA1/IO39RSB0
E8	GCA0/IO40RSB0
E9	GCB2/IO42RSB0
F1[1]	VCCPLF
F2[1]	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO49RSB0
F8	GDC1/IO45RSB0
F9	GDC0/IO46RSB0
G1	GEA0/IO69RSB1
G2	GEC1/IO74RSB1
G3	GEB1/IO72RSB1
G4	IO63RSB1
G5	IO60RSB1
G6	IO54RSB1
G7	GDB2/IO52RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO70RSB1
H2	FF/GEB2/IO67RSB1
H3	IO65RSB1
H4	IO62RSB1
H5	IO59RSB1
H6	IO56RSB1
H7[2]	GDA2/IO51RSB1
H8	TDI
H9	TDO
J1	GEA2/IO68RSB1
J2	GEC2/IO66RSB1
J3	IO64RSB1
J4	IO61RSB1
J5	IO58RSB1
J6	IO55RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	**AGLN060Z Function**
A1	GAA0/IO02RSB0
A2	GAA1/IO03RSB0
A3	GAC0/IO06RSB0
A4	IO09RSB0
A5	IO13RSB0
A6	IO18RSB0
A7	GBB0/IO21RSB0
A8	GBA1/IO24RSB0
A9	GBA2/IO25RSB0
B1	GAA2/IO95RSB1
B2	GAB0/IO04RSB0
B3	GAC1/IO07RSB0
B4	IO08RSB0
B5	IO15RSB0
B6	GBC0/IO19RSB0
B7	GBB1/IO22RSB0
B8	IO26RSB0
B9	GBB2/IO27RSB0
C1	GAB2/IO93RSB1
C2	IO94RSB1
C3	GND
C4	IO10RSB0
C5	IO17RSB0
C6	GND
C7	GBA0/IO23RSB0
C8	GBC2/IO29RSB0
C9	IO31RSB0
D1	GAC2/IO91RSB1
D2	IO92RSB1
D3	GFA2/IO80RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO43RSB0
D8	GCC1/IO35RSB0
D9	GCC0/IO36RSB0
E1	GFB0/IO83RSB1
E2	GFB1/IO84RSB1
E3	GFA1/IO81RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0

CS81	
Pin Number	**AGLN060Z Function**
E7	GCA1/IO39RSB0
E8	GCA0/IO40RSB0
E9	GCB2/IO42RSB0
F1[1]	VCCPLF
F2[1]	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO49RSB0
F8	GDC1/IO45RSB0
F9	GDC0/IO46RSB0
G1	GEA0/IO69RSB1
G2	GEC1/IO74RSB1
G3	GEB1/IO72RSB1
G4	IO63RSB1
G5	IO60RSB1
G6	IO54RSB1
G7	GDB2/IO52RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO70RSB1
H2	FF/GEB2/IO67RSB1
H3	IO65RSB1
H4	IO62RSB1
H5	IO59RSB1
H6	IO56RSB1
H7[2]	GDA2/IO51RSB1
H8	TDI
H9	TDO
J1	GEA2/IO68RSB1
J2	GEC2/IO66RSB1
J3	IO64RSB1
J4	IO61RSB1
J5	IO58RSB1
J6	IO55RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	**AGLN125 Function**
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO13RSB0
A5	IO22RSB0
A6	IO32RSB0
A7	GBB0/IO37RSB0
A8	GBA1/IO40RSB0
A9	GBA2/IO41RSB0
B1	GAA2/IO132RSB1
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO11RSB0
B5	IO25RSB0
B6	GBC0/IO35RSB0
B7	GBB1/IO38RSB0
B8	IO42RSB0
B9	GBB2/IO43RSB0
C1	GAB2/IO130RSB1
C2	IO131RSB1
C3	GND
C4	IO15RSB0
C5	IO28RSB0
C6	GND
C7	GBA0/IO39RSB0
C8	GBC2/IO45RSB0
C9	IO47RSB0
D1	GAC2/IO128RSB1
D2	IO129RSB1
D3	GFA2/IO117RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO59RSB0
D8	GCC1/IO51RSB0
D9	GCC0/IO52RSB0
E1	GFB0/IO120RSB1
E2	GFB1/IO121RSB1
E3	GFA1/IO118RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0

CS81	
Pin Number	**AGLN125 Function**
E7	GCA0/IO56RSB0
E8	GCA1/IO55RSB0
E9	GCB2/IO58RSB0
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO65RSB0
F8	GDC1/IO61RSB0
F9	GDC0/IO62RSB0
G1	GEA0/IO104RSB1
G2	GEC0/IO108RSB1
G3	GEB1/IO107RSB1
G4	IO96RSB1
G5	IO92RSB1
G6	IO72RSB1
G7	GDB2/IO68RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO105RSB1
H2	FF/GEB2/IO102RSB1
H3	IO99RSB1
H4	IO94RSB1
H5	IO91RSB1
H6	IO81RSB1
H7	GDA2/IO67RSB1
H8	TDI
H9	TDO
J1	GEA2/IO103RSB1
J2	GEC2/IO101RSB1
J3	IO97RSB1
J4	IO93RSB1
J5	IO90RSB1
J6	IO78RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	**AGLN125Z Function**
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO13RSB0
A5	IO22RSB0
A6	IO32RSB0
A7	GBB0/IO37RSB0
A8	GBA1/IO40RSB0
A9	GBA2/IO41RSB0
B1	GAA2/IO132RSB1
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO11RSB0
B5	IO25RSB0
B6	GBC0/IO35RSB0
B7	GBB1/IO38RSB0
B8	IO42RSB0
B9	GBB2/IO43RSB0
C1	GAB2/IO130RSB1
C2	IO131RSB1
C3	GND
C4	IO15RSB0
C5	IO28RSB0
C6	GND
C7	GBA0/IO39RSB0
C8	GBC2/IO45RSB0
C9	IO47RSB0
D1	GAC2/IO128RSB1
D2	IO129RSB1
D3	GFA2/IO117RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	GCC2/IO59RSB0
D8	GCC1/IO51RSB0
D9	GCC0/IO52RSB0
E1	GFB0/IO120RSB1
E2	GFB1/IO121RSB1
E3	GFA1/IO118RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0

CS81	
Pin Number	**AGLN125Z Function**
E7	GCA0/IO56RSB0
E8	GCA1/IO55RSB0
E9	GCB2/IO58RSB0
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB1
F6	GND
F7	GDA1/IO65RSB0
F8	GDC1/IO61RSB0
F9	GDC0/IO62RSB0
G1	GEA0/IO104RSB1
G2	GEC0/IO108RSB1
G3	GEB1/IO107RSB1
G4	IO96RSB1
G5	IO92RSB1
G6	IO72RSB1
G7	GDB2/IO68RSB1
G8	VJTAG
G9	TRST
H1	GEA1/IO105RSB1
H2	FF/GEB2/IO102RSB1
H3	IO99RSB1
H4	IO94RSB1
H5	IO91RSB1
H6	IO81RSB1
H7	GDA2/IO67RSB1
H8	TDI
H9	TDO
J1	GEA2/IO103RSB1
J2	GEC2/IO101RSB1
J3	IO97RSB1
J4	IO93RSB1
J5	IO90RSB1
J6	IO78RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81	
Pin Number	AGLN250 Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO12RSB0
A7	GBB0/IO16RSB0
A8	GBA1/IO19RSB0
A9	GBA2/IO20RSB1
B1	GAA2/IO67RSB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO06RSB0
B5	IO10RSB0
B6	GBC0/IO14RSB0
B7	GBB1/IO17RSB0
B8	IO21RSB1
B9	GBB2/IO22RSB1
C1	GAB2/IO65RSB3
C2	IO66RSB3
C3	GND
C4	IO08RSB0
C5	IO11RSB0
C6	GND
C7	GBA0/IO18RSB0
C8	GBC2/IO23RSB1
C9	IO24RSB1
D1	GAC2/IO63RSB3
D2	IO64RSB3
D3	GFA2/IO56RSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO30RSB1
D8	GCC1/IO25RSB1
D9	GCC0/IO26RSB1
E1	GFB0/IO59RSB3
E2	GFB1/IO60RSB3
E3	GFA1/IO58RSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1

CS81	
Pin Number	AGLN250 Function
E7	GCA0/IO28RSB1
E8	GCA1/IO27RSB1
E9	GCB2/IO29RSB1
F1	VCCPLF
F2	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO33RSB1
F8	GDC1/IO31RSB1
F9	GDC0/IO32RSB1
G1	GEA0/IO51RSB3
G2	GEC1/IO54RSB3
G3	GEC0/IO53RSB3
G4	IO45RSB2
G5	IO42RSB2
G6	IO37RSB2
G7	GDB2/IO35RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO52RSB3
H2	FF/GEB2/IO49RSB2
H3	IO47RSB2
H4	IO44RSB2
H5	IO41RSB2
H6	IO39RSB2
H7	GDA2/IO34RSB2
H8	TDI
H9	TDO
J1	GEA2/IO50RSB2
J2	GEC2/IO48RSB2
J3	IO46RSB2
J4	IO43RSB2
J5	IO40RSB2
J6	IO38RSB2
J7	TCK
J8	TMS
J9	VPUMP

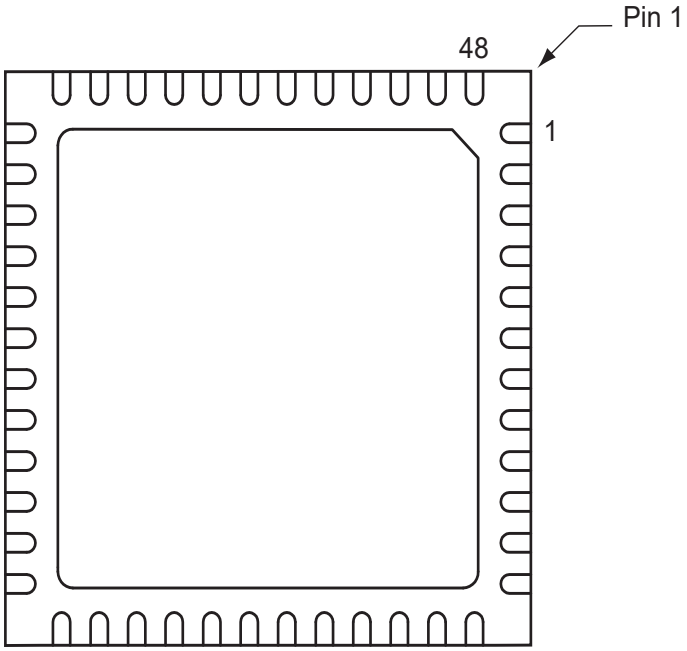
CS81	
Pin Number	AGLN250Z Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO12RSB0
A7	GBB0/IO16RSB0
A8	GBA1/IO19RSB0
A9	GBA2/IO20RSB1
B1	GAA2/IO67RSB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO06RSB0
B5	IO10RSB0
B6	GBC0/IO14RSB0
B7	GBB1/IO17RSB0
B8	IO21RSB1
B9	GBB2/IO22RSB1
C1	GAB2/IO65RSB3
C2	IO66RSB3
C3	GND
C4	IO08RSB0
C5	IO11RSB0
C6	GND
C7	GBA0/IO18RSB0
C8	GBC2/IO23RSB1
C9	IO24RSB1
D1	GAC2/IO63RSB3
D2	IO64RSB3
D3	GFA2/IO56RSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO30RSB1
D8	GCC1/IO25RSB1
D9	GCC0/IO26RSB1
E1	GFB0/IO59RSB3
E2	GFB1/IO60RSB3
E3	GFA1/IO58RSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1

CS81	
Pin Number	**AGLN250Z Function**
E7	GCA0/IO28RSB1
E8	GCA1/IO27RSB1
E9	GCB2/IO29RSB1
F1*	VCCPLF
F2*	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO33RSB1
F8	GDC1/IO31RSB1
F9	GDC0/IO32RSB1
G1	GEA0/IO51RSB3
G2	GEC1/IO54RSB3
G3	GEC0/IO53RSB3
G4	IO45RSB2
G5	IO42RSB2
G6	IO37RSB2
G7	GDB2/IO35RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO52RSB3
H2	FF/GEB2/IO49RSB2
H3	IO47RSB2
H4	IO44RSB2
H5	IO41RSB2
H6	IO39RSB2
H7	GDA2/IO34RSB2
H8	TDI
H9	TDO
J1	GEA2/IO50RSB2
J2	GEC2/IO48RSB2
J3	IO46RSB2
J4	IO43RSB2
J5	IO40RSB2
J6	IO38RSB2
J7	TCK
J8	TMS
J9	VPUMP

4.4 QN48

This is the bottom view of the QN48 package

FIGURE 4-4: QN48



Note 1: The die attach paddle of the package is tied to ground (GND).

2: For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/support/package-drawings/fpga-packaging.

3: Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN060-CS81.

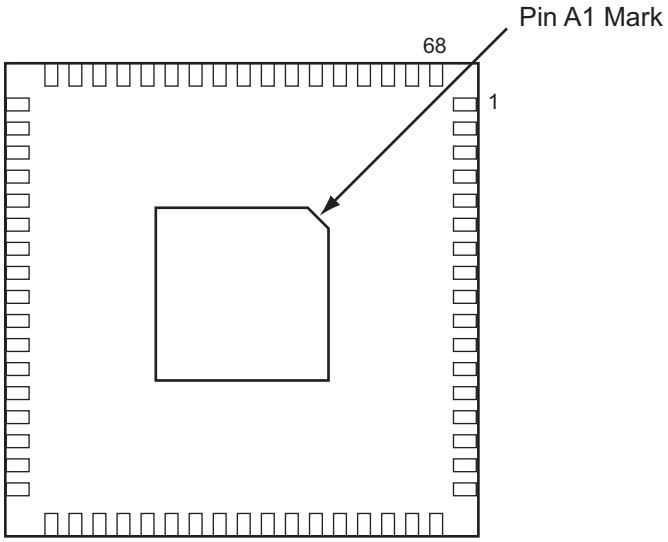
4: The bus hold attribute (hold previous I/O state in Flash*Freeze mode) is not supported for pin H7 in AGLN060-CS81.

QN48	
Pin Number	**AGLN030Z Function**
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	FF/IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

4.5 QN68

This is the bottom view of the QN68 package.

FIGURE 4-5: QN68



Note 1: The die attach paddle of the package is tied to ground (GND).

2: For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/support/package-drawings/fpga-packaging.

3: Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN125-CS81.

QN68	
Pin Number	**AGLN015 Function**
1	IO60RSB2
2	IO54RSB2
3	IO52RSB2
4	IO50RSB2
5	IO49RSB2
6	GEC0/IO48RSB2
7	GEA0/IO47RSB2
8	VCC
9	GND
10	VCCIB2
11	IO46RSB2
12	IO45RSB2
13	IO44RSB2
14	IO43RSB2
15	IO42RSB2
16	IO41RSB2
17	IO40RSB2
18	FF/IO39RSB1
19	IO37RSB1
20	IO35RSB1
21	IO33RSB1
22	IO31RSB1
23	IO30RSB1
24	VCC
25	GND
26	VCCIB1
27	IO27RSB1
28	IO25RSB1
29	IO23RSB1
30	IO21RSB1
31	IO19RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO17RSB0
40	IO16RSB0
41	GDA0/IO15RSB0

QN68	
Pin Number	**AGLN015 Function**
42	GDC0/IO14RSB0
43	IO13RSB0
44	VCCIB0
45	GND
46	VCC
47	IO12RSB0
48	IO11RSB0
49	IO09RSB0
50	IO05RSB0
51	IO00RSB0
52	IO07RSB0
53	IO03RSB0
54	IO18RSB1
55	IO20RSB1
56	IO22RSB1
57	IO24RSB1
58	IO28RSB1
59	NC
60	GND
61	NC
62	IO32RSB1
63	IO34RSB1
64	IO36RSB1
65	IO61RSB2
66	IO58RSB2
67	IO56RSB2
68	IO63RSB2

QN68	
Pin Number	**AGLN020 Function**
1	IO60RSB2
2	IO54RSB2
3	IO52RSB2
4	IO50RSB2
5	IO49RSB2
6	GEC0/IO48RSB2
7	GEA0/IO47RSB2
8	VCC
9	GND
10	VCCIB2

QN68	
Pin Number	**AGLN020 Function**
11	IO46RSB2
12	IO45RSB2
13	IO44RSB2
14	IO43RSB2
15	IO42RSB2
16	IO41RSB2
17	IO40RSB2
18	FF/IO39RSB1
19	IO37RSB1
20	IO35RSB1
21	IO33RSB1
22	IO31RSB1
23	IO30RSB1
24	VCC
25	GND
26	VCCIB1
27	IO27RSB1
28	IO25RSB1
29	IO23RSB1
30	IO21RSB1
31	IO19RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO17RSB0
40	IO16RSB0
41	GDA0/IO15RSB0
42	GDC0/IO14RSB0
43	IO13RSB0
44	VCCIB0
45	GND
46	VCC
47	IO12RSB0
48	IO11RSB0
49	IO09RSB0
50	IO05RSB0
51	IO00RSB0
52	IO07RSB0

QN68	
Pin Number	AGLN020 Function
53	IO03RSB0
54	IO18RSB1
55	IO20RSB1
56	IO22RSB1
57	IO24RSB1
58	IO28RSB1
59	NC
60	GND
61	NC
62	IO32RSB1
63	IO34RSB1
64	IO36RSB1
65	IO61RSB2
66	IO58RSB2
67	IO56RSB2
68	IO63RSB2

QN68	
Pin Number	AGLN030Z Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1

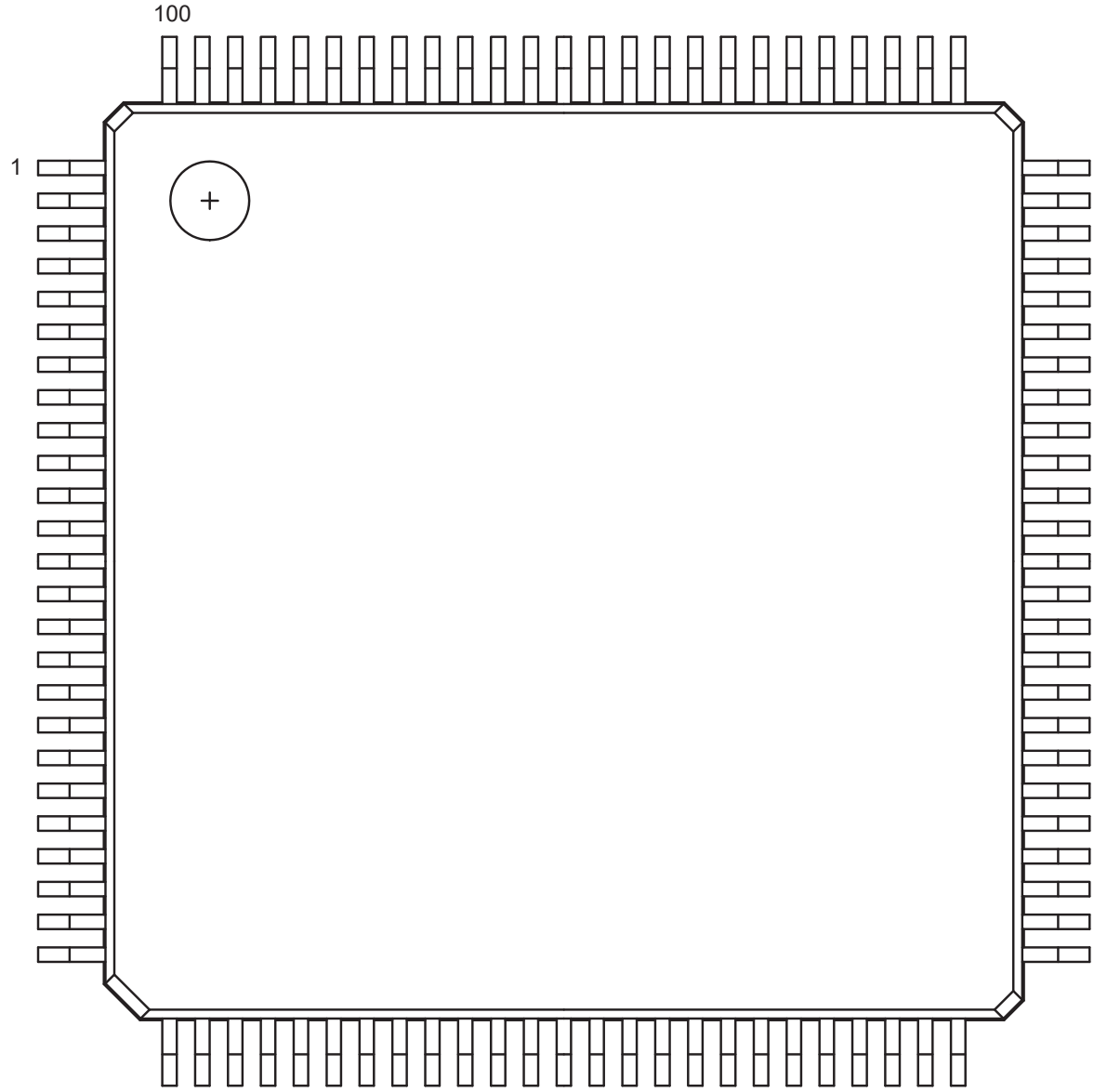
QN68	
Pin Number	AGLN030Z Function
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0

QN68	
Pin Number	AGLN030Z Function
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

4.6 VQ100

This is the top view of the VQ100 package.

FIGURE 4-6: VQ100



Note 1: For Package Manufacturing and Environmental information, visit the Resource Center at https://www.microchip.com/en-us/support/package-drawings/fpga-packaging.

2: Pin numbers F1 and F2 must be connected to ground because a PLL is not supported for AGLN250-CS81.

VQ100	
Pin Number	AGLN030Z Function
1	GND
2	IO82RSB1
3	IO81RSB1
4	IO80RSB1
5	IO79RSB1
6	IO78RSB1
7	IO77RSB1
8	IO76RSB1
9	GND
10	IO75RSB1
11	IO74RSB1
12	GEC0/IO73RSB1
13	GEA0/IO72RSB1
14	GEB0/IO71RSB1
15	IO70RSB1
16	IO69RSB1
17	VCC
18	VCCIB1
19	IO68RSB1
20	IO67RSB1
21	IO66RSB1
22	IO65RSB1
23	IO64RSB1
24	IO63RSB1
25	IO62RSB1
26	IO61RSB1
27	FF/IO60RSB1
28	IO59RSB1
29	IO58RSB1
30	IO57RSB1
31	IO56RSB1
32	IO55RSB1
33	IO54RSB1
34	IO53RSB1
35	IO52RSB1
36	IO51RSB1
37	VCC
38	GND
39	VCCIB1
40	IO49RSB1
41	IO47RSB1

VQ100	
Pin Number	AGLN030Z Function
42	IO46RSB1
43	IO45RSB1
44	IO44RSB1
45	IO43RSB1
46	IO42RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	IO41RSB0
58	IO40RSB0
59	IO39RSB0
60	IO38RSB0
61	IO37RSB0
62	IO36RSB0
63	GDB0/IO34RSB0
64	GDA0/IO33RSB0
65	GDC0/IO32RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	IO30RSB0
71	IO29RSB0
72	IO28RSB0
73	IO27RSB0
74	IO26RSB0
75	IO25RSB0
76	IO24RSB0
77	IO23RSB0
78	IO22RSB0
79	IO21RSB0
80	IO20RSB0
81	IO19RSB0
82	IO18RSB0
83	IO17RSB0

VQ100	
Pin Number	AGLN030Z Function
84	IO16RSB0
85	IO15RSB0
86	IO14RSB0
87	VCCIB0
88	GND
89	VCC
90	IO12RSB0
91	IO10RSB0
92	IO08RSB0
93	IO07RSB0
94	IO06RSB0
95	IO05RSB0
96	IO04RSB0
97	IO03RSB0
98	IO02RSB0
99	IO01RSB0
100	IO00RSB0

VQ100	
Pin Number	AGLN060 Function
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1

VQ100	
Pin Number	**AGLN060 Function**
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45*	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0

VQ100	
Pin Number	**AGLN060 Function**
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

VQ100	
Pin Number	**AGLN060Z Function**
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1

VQ100	
Pin Number	**AGLN060Z Function**
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1
36	IO61RSB1
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45*	GDB2/IO55RSB1
46	GDA2/IO54RSB1

VQ100	
Pin Number	AGLN060Z Function
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC

VQ100	
Pin Number	AGLN060Z Function
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

VQ100	
Pin Number	AGLN125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1

VQ100	
Pin Number	AGLN125 Function
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0

VQ100	
Pin Number	AGLN125 Function
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

VQ100	
Pin Number	AGLN125Z Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI

VQ100	
Pin Number	AGLN125Z Function
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0

VQ100	
Pin Number	AGLN125Z Function
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

VQ100	
Pin Number	AGLN250 Function
1	GND
2	GAA2/IO67RSB3
3	IO66RSB3
4	GAB2/IO65RSB3
5	IO64RSB3
6	GAC2/IO63RSB3
7	IO62RSB3
8	IO61RSB3
9	GND
10	GFB1/IO60RSB3
11	GFB0/IO59RSB3
12	VCOMPLF
13	GFA0/IO57RSB3
14	VCCPLF
15	GFA1/IO58RSB3
16	GFA2/IO56RSB3
17	VCC
18	VCCIB3
19	GFC2/IO55RSB3
20	GEC1/IO54RSB3
21	GEC0/IO53RSB3
22	GEA1/IO52RSB3
23	GEA0/IO51RSB3
24	VMV3
25	GNDQ
26	GEA2/IO50RSB2
27	FF/GEB2/IO49RSB2
28	GEC2/IO48RSB2

VQ100	
Pin Number	AGLN250 Function
29	IO47RSB2
30	IO46RSB2
31	IO45RSB2
32	IO44RSB2
33	IO43RSB2
34	IO42RSB2
35	IO41RSB2
36	IO40RSB2
37	VCC
38	GND
39	VCCIB2
40	IO39RSB2
41	IO38RSB2
42	IO37RSB2
43	GDC2/IO36RSB2
44	GDB2/IO35RSB2
45	GDA2/IO34RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO33RSB1
58	GDC0/IO32RSB1
59	GDC1/IO31RSB1
60	IO30RSB1
61	GCB2/IO29RSB1
62	GCA1/IO27RSB1
63	GCA0/IO28RSB1
64	GCC0/IO26RSB1
65	GCC1/IO25RSB1
66	VCCIB1
67	GND
68	VCC
69	IO24RSB1
70	GBC2/IO23RSB1
71	GBB2/IO22RSB1

VQ100	
Pin Number	AGLN250 Function
72	IO21RSB1
73	GBA2/IO20RSB1
74	VMV1
75	GNDQ
76	GBA1/IO19RSB0
77	GBA0/IO18RSB0
78	GBB1/IO17RSB0
79	GBB0/IO16RSB0
80	GBC1/IO15RSB0
81	GBC0/IO14RSB0
82	IO13RSB0
83	IO12RSB0
84	IO11RSB0
85	IO10RSB0
86	IO09RSB0
87	VCCIB0
88	GND
89	VCC
90	IO08RSB0
91	IO07RSB0
92	IO06RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

VQ100	
Pin Number	AGLN250Z Function
1	GND
2	GAA2/IO67RSB3
3	IO66RSB3
4	GAB2/IO65RSB3
5	IO64RSB3
6	GAC2/IO63RSB3
7	IO62RSB3
8	IO61RSB3
9	GND
10	GFB1/IO60RSB3

VQ100	
Pin Number	AGLN250Z Function
11	GFB0/IO59RSB3
12	VCOMPLF
13	GFA0/IO57RSB3
14	VCCPLF
15	GFA1/IO58RSB3
16	GFA2/IO56RSB3
17	VCC
18	VCCIB3
19	GFC2/IO55RSB3
20	GEC1/IO54RSB3
21	GEC0/IO53RSB3
22	GEA1/IO52RSB3
23	GEA0/IO51RSB3
24	VMV3
25	GNDQ
26	GEA2/IO50RSB2
27	FF/GEB2/IO49RSB2
28	GEC2/IO48RSB2
29	IO47RSB2
30	IO46RSB2
31	IO45RSB2
32	IO44RSB2
33	IO43RSB2
34	IO42RSB2
35	IO41RSB2
36	IO40RSB2
37	VCC
38	GND
39	VCCIB2
40	IO39RSB2
41	IO38RSB2
42	IO37RSB2
43	GDC2/IO36RSB2
44	GDB2/IO35RSB2
45	GDA2/IO34RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC

VQ100	
Pin Number	AGLN250Z Function
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO33RSB1
58	GDC0/IO32RSB1
59	GDC1/IO31RSB1
60	IO30RSB1
61	GCB2/IO29RSB1
62	GCA1/IO27RSB1
63	GCA0/IO28RSB1
64	GCC0/IO26RSB1
65	GCC1/IO25RSB1
66	VCCIB1
67	GND
68	VCC
69	IO24RSB1
70	GBC2/IO23RSB1
71	GBB2/IO22RSB1
72	IO21RSB1
73	GBA2/IO20RSB1
74	VMV1
75	GNDQ
76	GBA1/IO19RSB0
77	GBA0/IO18RSB0
78	GBB1/IO17RSB0
79	GBB0/IO16RSB0
80	GBC1/IO15RSB0
81	GBC0/IO14RSB0
82	IO13RSB0
83	IO12RSB0
84	IO11RSB0
85	IO10RSB0
86	IO09RSB0
87	VCCIB0
88	GND
89	VCC
90	IO08RSB0
91	IO07RSB0
92	IO06RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0

VQ100	
Pin Number	AGLN250Z Function
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

5.0 RELATED DOCUMENTS

5.1 User Guides

IGLOO nano FPGA Fabric User's Guide

5.2 Packaging Documents

The following documents provide packaging information and device selection for low power Flash devices.

5.2.1 PRODUCT CATALOG

FPGA and SoC Product Catalog

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

5.2.2 *PACKAGE MECHANICAL DRAWINGS*

This document contains the package mechanical drawings for all packages currently or previously supplied by Microchip. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are on the Microchip SoC Products Group website: https://www.microchip.com/en-us/support/package-drawings/fpga-packaging.

APPENDIX A: REVISION HISTORY

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

A.1 Revision A: March 2024

The following is a list of changes that were made in revision A of the datasheet:

- Migrated the document to Microchip template.
- Modified the document by adding the references to AGLN015. AGLN015 device was mistakenly removed in the previous version. Hence, it was added back in this version.
- The document number has been updated to DS50003670A.
- Updated the following tables to include AGLN015 device which was removed in the previous revision: – *Table 1*, *Table 2*, *Table 4*, and *Table 5*.
- Added table note stating “Not recommended for new designs. (CN1203)” in *Table 1* and *Table 2*.
- Updated *Figure 1* to include AGLN015 device.

A.2 Revision 20: October 2019

The following list of changes that were made in revision A of the datasheet.

- Modified *Table 1* by removing references to AGLN015.
- Modified the *Table 2* by removing references to AGLN015.
- Modified the *"IGLOO nano Device Status"* section.
- Modified the *"IGLOO nano Ordering Information"* section by removing references to AGLN015.
- Removed the "Devices Not Recommended For New Designs" section.
- Modified the *"Device Marking"* section.
- Removed the "IGLOO nano Products Available in the Z Feature Grade" section.
- Modified the *"Temperature Grade Offerings"* section.
- Removed reference of AGLN015 from the *Figure 1-2*.
- Modified *Table 2-9* table by removing references to AGLN015.
- Modified *Table 2-10* table by removing references to AGLN015.
- Modified *Table 2-11* table by removing references to AGLN015.
- Modified *Table 2-12* table by removing references to AGLN015.
- Modified *Table 2-15* table by removing references to AGLN015.
- Modified *Table 2-16* table by removing references to AGLN015.
- Modified *Table 2-17* table by removing references to AGLN015.
- Modified *Table 2-18* table by removing references to AGLN015.
- Modified the note under *Section 2.3.6, DDR Module Specifications* by removing reference to AGLN015.
- Modified the *Section 2.5.2, Global Tree Timing Characteristics* section by removing references to AGLN015.
- Modified the notes in the *Section 2.6, Clock Conditioning Circuits* section by removing reference to AGLN015.
- Modified *Section 4.2, UC81*.
- Modified *Section 4.3, CS81*.
- Modified *Section 4.4, QN48*.
- Modified *Section 4.5, QN68*
- Modified *Section 4.6, VQ100*.

A.3 Revision 19 - October 2015

The following list of changes that were made in revision 19 of the datasheet.

- Modified the note to include device/package obsoletion information in *"Features"*.
- Added a note under Security Feature "Y" in *"IGLOO nano Ordering Information"*.
- Modified AGLN250 pin assignment table to match with I/O Attribute Editor tool from Libero in *"CS81"* Package.
- Modified the nominal area to 25 for CS81 Package in *Table 3*.

- Modified the title of AGLN125Z pin assignment table for *"CS81"* Package.

A.4 Revision 18 - November 2013

The following list of changes that were made in revision 18 of the datasheet:

- Modified the *"Device Marking"* and updated *Figure 2* to reflect updates suggested per CN1004 published on 5/10/2010.

A.5 Revision 17 - May 2013

The following list of changes that were made in revision 17 of the datasheet:

- Deleted details related to Ambient temperature from *"Enhanced Commercial Temperature Range"*, *"IGLOO nano Ordering Information"*, *"Temperature Grade Offerings"*, and *Table 2-2* to remove ambiguities arising due to the same, and modified Note 2.

A.6 Revision 16 - December 2012

The following list of changes that were made in revision 16 of the datasheet:

- The *"IGLOO nano Ordering Information"* has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio".
- The note in *Table 2-100* and *Table 2-101* referring the reader to SmartGen was revised to refer instead to the online help associated with the core.
- Live at Power-Up (LAPU) has been replaced with 'Instant On'.

A.7 Revision 15 - September 2012

The following list of changes that were made in revision 15 of the datasheet:

- The status of the AGLN125 device has been modified from 'Advance' to 'Production' in the *"IGLOO nano Device Status"* section.
- Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document.

A.8 Revision 14 - September 2012

The following list of changes that were made in revision 14 of the datasheet.

- The *"Security"* section was modified to clarify that Microchip does not support read-back of programmed data.

A.9 Revision 13 - June 2012

The following list of changes that were made in revision 13 of the datasheet:

- *Figure 2-34* and *Figure 2-35* have been added.
- The following sentence was removed from the *"VMVx —I/O Supply Voltage (quiet)"* in the *"Pin Descriptions"*: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks". The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.

A.10 Revision 12 - March 2012

The following list of changes that were made in revision 12 of the datasheet:

- The *"In-System Programming (ISP) and Security"* and *"Security"* were revised to clarify that although no existing security measures can give an absolute guarantee, Microchip FPGAs implement the best security available in the industry.
- Notes indicating that AGLN015 is not recommended for new designs have been added.
- Notes indicating that nano-Z devices are not recommended for new designs have been added. The "Devices Not Recommended For New Designs" is new.
- The Y security option and Licensed DPA Logo were added to the *"IGLOO nano Ordering Information"*. The trade-

marked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research.

- The following sentence was removed from the *"Advanced Architecture"*: "In addition, extensive on-chip programming circuitry enables rapid, single-voltage (3.3V) programming of IGLOO nano devices through an IEEE 1532 JTAG interface".
- The *"Specifying I/O States During Programming"* is new.
- The reference to guidelines for global spines and VersaTile rows, given in the *"Global Clock Contribution—PCLOCK"*, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *IGLOO nano FPGA Fabric User's Guide*.
- *Figure 2-4* has been modified for DIN waveform; the Rise and Fall time label has been changed to tDIN (37106).
- The AC Loading figures in the *"Single-Ended I/O Characteristics"* were updated to match tables in the *"Summary of I/O Timing Characteristics – Default I/O Software Settings"* .
- The notes regarding drive strength in the *"Summary of I/O Timing Characteristics – Default I/O Software Settings"*, *"3.3V LVCMOS Wide Range"* and *"1.2V LVCMOS Wide Range"* tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, see the IBIS models.
- Added values for minimum pulse width and removed the FRMAX row from *Table 2-88* through *Table 2-99* in the *"Global Tree Timing Characteristics"*. Use the software to determine the FRMAX for the device you are using.
- *Table 2-100* and *Table 2-101* were updated. A note was added indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available.
- The port names in the SRAM *"Timing Waveforms for Embedded SRAM"*, SRAM *"Timing Characteristics: 1.5V DC Core Voltage"* tables, *Figure 2-36*, and the FIFO *"Timing Characteristics: 1.5V DC Core Voltage"* tables were revised to ensure consistency with the software names.
- Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 34865).
- The *"Pin Descriptions"* chapter has been added.
- Package names used in the *"Package Pin Assignments"* were revised to match standards given in *Package Mechanical Drawings*.

A.11 Revision 11 - Jul 2010

The following list of changes that were made in revision 11 of the datasheet:

- The status of the AGLN060 device has changed from Advance to Production.
- The values for PAC1, PAC2, PAC3, and PAC4 were updated in *Table 2-15* for 1.5V core supply voltage.
- The values for PAC1, PAC2, PAC3, and PAC4 were updated in *Table 2-17* for 1.2 V core supply voltage.
- The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The *"IGLOO nano Device Status"* indicates the status for each device in the device family.

A.12 Revision 10 - April 2010

The following list of changes that were made in revision 10 of the datasheet:

- References to differential inputs were removed from the datasheet, since IGLOO nano devices do not support differential inputs.
- A parenthetical note, "hold previous I/O state in Flash*Freeze mode," was added to each occurrence of bus hold in the datasheet.
- The *"In-System Programming (ISP) and Security"* was revised to add 1.2V programming.
- The note connected with the *"IGLOO nano Ordering Information"* was revised to clarify features not available for Z feature grade devices.
- The *"IGLOO nano Device Status"* is new.
- The definition of C in the *"Temperature Grade Offerings"* was changed to "extended commercial temperature range".
- 1.2V wide range was added to the list of voltage ranges in the *"I/Os with Advanced I/O Standards"*.
- A note was added to *Table 2-2* regarding switching from 1.2V to 1.5V core voltage for in-system programming.

The VJTAG voltage was changed from "1.425 to 3.6" to "1.4 to 3.6". The note regarding voltage for programming V2 and V5 devices was revised. The maximum value for VPUMP programming voltage (operation mode) was changed from 3.45V to 3.6V.

- *Table 2-6* and *Table 2-7* were updated. *Table 2-8* is new.
- The tables in the *"Quiescent Supply Current"* were updated.
- VJTAG was removed from *Table 2-10*.
- The note stating what was included in I_{DD} was removed from *Table 2-11*. The note, "per VCCI or VJTAG bank" was removed from *Table 2-12*. The note giving I_{DD} was changed to "$I_{DD} = N_{BANKS} * I_{CCI} + I_{CCA}$."
- The values in *Table 2-13* and *Table 2-14* were updated. Wide range support information was added.
- The following tables were updated with current available information. The equivalent software default drive strength option was added:
  - *Table 2-21*
  - *Table 2-25*
  - *Table 2-26*
  - *Table 2-28*
  - *Table 2-29*
  - *Table 2-30*
- Timing tables in the *"Single-Ended I/O Characteristics"*, including new tables for 3.3V and 1.2V LVCMOS wide range.
  - *Table 2-40*
  - *Table 2-63*
  - *Table 2-67* (new)
- The formulas in the notes to *Table 2-29* were revised.
- The text introducing *Table 2-31* was revised to state six months at 100° instead of three months at 110° for reliability concerns. The row for 110° was removed from the table.
- The following sentence was deleted from the *"2.5V LVCMOS"*: "It uses a 5V tolerant input buffer and push-pull output buffer."
- The $F_{DDRIMAX}$ and F_{DDOMAX} values were added to tables in the *"DDR Module Specifications"*. A note was added stating that DDR is not supported for AGLN010, AGLN015, and AGLN020.
- Tables in the *"Global Tree Timing Characteristics"* were updated with new information available.
- *Table 2-100* and *Table 2-101* were revised.
- Tables in the SRAM *"Timing Characteristics: 1.5V DC Core Voltage"* and FIFO *"Timing Characteristics: 1.5V DC Core Voltage"* were updated with new information available.
- *Table 3-3* is new.
- A note was added to the *"CS81"* pin tables for AGLN060, AGLN060Z, AGLN125, AGLN125Z, AGLN250, and AGLN250Z indicating that pins F1 and F2 must be grounded.
- A note was added to the *"CS81"* and *"VQ100"* pin tables for AGLN060 and AGLN060Z stating that bus hold is not available for pin H7 or pin 45.
- The AGLN250 function for pin C8 in the *"CS81"* table was revised.

A.13 Revision 9 (Product Brief Advance v0.9 Packaging Advance v0.8)- March 2010

The following list of changes that were made in revision 9 of the datasheet:

- All product tables and pin tables were updated to show clearly that AGLN030 is available only in the Z feature grade at this time. The nano-Z feature grade devices are designated with a Z at the end of the part number.

A.14 Revision 8 (Product Brief Advance v0.8 and Packaging Advance v0.7)- January 2009

The following list of changes that were made in revision 8 of the datasheet:

- The *"Reprogrammable Flash Technology"* was revised to add "250 MHz (1.5V systems) and 160 MHz (1.2V systems) System Performance".
- The note for AGLN030 in the *"IGLOO nano Devices"* table and *"I/Os Per Package"* table was revised to remove the statement regarding package compatibility with lower density nano devices.

- The *"I/Os with Advanced I/O Standards"* was revised to add definitions for hot-swap and cold-sparing.
- The *"UC81"*, *"CS81"*, *"QN48"*, and *"QN68"* pin tables for AGLN030 are new.
- The *"CS81"* pin table for AGLN060 is new.
- The *"CS81"* and *"VQ100"* pin tables for AGLN060Z are new.
- The *"CS81"* and *"VQ100"* pin tables for AGLN125Z are new.
- The *"CS81"* and *"VQ100"* pin tables for AGLN250Z is new.

A.15 Revision 7 (Product Brief Advance v0.7 and DC and Switching Characteristics Advance v0.3) - April 2009

The following list of changes that were made in revision 7 of the datasheet:

- The –F speed grade is no longer offered for IGLOO nano devices and was removed from the datasheet.

A.16 Revision 6 - March 2009

The following list of changes that were made in revision 6 of the datasheet:

- The *"VQ100"* pin table for AGLN030 is new.

A.17 Revision 5 (Packaging Advance v0.5) - Feb 2009

The following list of changes that were made in revision 5 of the datasheet:

- The "100-Pin QFN" section was removed.

A.18 Revision 4 (Product Brief Advance v0.6) - Feb 2009

The following list of changes that were made in revision 4 of the datasheet:

- The QN100 package was removed for all devices.
- *"IGLOO nano Devices"* was updated to change the maximum user I/Os for AGLN030 from 81 to 77.
- The *"Device Marking"* is new.

A.19 Revision 3 (Product Brief Advance v0.5) - Feb 2009

The following list of changes that were made in revision 3 of the datasheet.

- The following table note was removed from *"IGLOO nano Devices"*: "Six chip (main) and three quadrant global networks are available for AGLN060 and above."
- The CS81 package was added for AGLN250 in the "IGLOO nano Products Available in the Z Feature Grade" table.
- The *"UC81"* and *"CS81"* pin tables for AGLN020 are new.
- The *"CS81"* pin table for AGLN250 is new.

A.20 Revision 2 (Product Brief Advance v0.4 and Packaging Advance v0.3) - December 2008

The following list of changes that were made in revision 2 of the datasheet.

- The second table note in *"IGLOO nano Devices"* was revised to state, "AGLN060, AGLN125, and AGLN250 in the CS81 package do not support PLLs. AGLN030 and smaller devices do not support this feature."
- The I/Os per package for CS81 were revised to 60 for AGLN060, AGLN125, and AGLN250 in the *"I/Os Per Package"* table.
- The *"UC36"* pin table is new.

A.21 Revision 1 (Product Brief Advance v0.3) - November 2008

- The following list of changes that were made in revision 1 of the datasheet.
- The *"Advanced I/Os"* was updated to include wide power supply voltage support for 1.14V to 1.575V.
- The AGLN030 device was added to product tables and replaces AGL030 entries that were formerly in the tables.

- The *"I/Os Per Package"* table was updated for the CS81 package to change the number of I/Os for AGLN060, AGLN125, and AGLN250 from 66 to 64.
- The *"Wide Range I/O Support"* is new.
- The table notes and references were revised in *Table 2-2*. VMV was included with VCCI and a table note was added stating, "VMV pins must be connected to the corresponding VCCI pins. See *Pin Descriptions* for further information." Please review carefully.
- VJTAG was added to the list in the table note for *Table 2-9*. Values were added for AGLN010, AGLN015, and AGLN030 for 1.5V.
- VCCI was removed from the list in the table note for *Table 2-10*.
- Values for I_{CCA} current were updated for AGLN010, AGLN015, and AGLN030 in *Table 2-12*.
- Values for PAC1 and PAC2 were added to *Table 2-15* and *Table 2-17*.
- Table notes regarding wide range support were added to *Table 2-21*.
- 1.2V LVCMOS wide range values were added to *Table 2-22* and *Table 2-23*.
- The following table note was added to *Table 2-25* and *Table 2-26*: "All LVCMOS 3.3V software macros support LVCMOS 3.3V wide range, as specified in the JESD8-B specification."
- 3.3 V LVCMOS Wide Range and 1.2V Wide Range were added to *Table 2-28* and *Table 2-30*.

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